EcoSpeed™ DC-DC Converter with Integrated Boost Diode

Features

- Power system
  - Input voltage — 3V to 28V
  - Integrated bootstrap switch
  - 1% reference tolerance -40 to +85 °C
  - EcoSpeed™ architecture with pseudo-fixed frequency adaptive on-time control
  - Internal soft-start and soft-shutdown at output
  - SmartDrive™
- Logic input/output control
  - Independent control EN for LDO and switcher
  - Programmable V_{IN} UVLO threshold
  - Power good output
  - Selectable power save mode
  - Programmable ultrasonic power save mode
- Protections
  - Over-voltage/under-voltage
  - TC compensated $R_{DS(ON)}$ sensed current limit
  - Thermal shutdown
  - Smart power save
- Output capacitor types
  - High ESR — SP, POSCAP, OSCON
  - Ceramic capacitors
- Package — 3 x 3mm, 20-pin MLPQ
- Lead-free and halogen free
- RoHS and WEEE compliant

Applications

- Office automation and computing
- Networking and telecommunication equipment
- Point-of-load power supplies and module replacement

Description

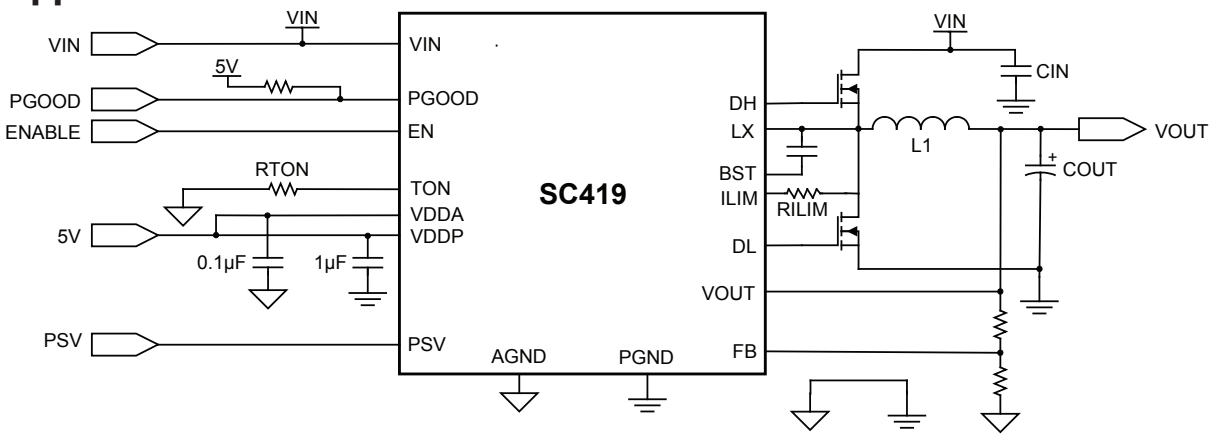
The SC419 is a synchronous buck power supply controller. It features a bootstrap switch in a space-saving MLPQ-3 x 3mm 20-pin package. The device is highly efficient and uses minimal PCB area. It uses pseudo-fixed frequency adaptive on-time operation to provide fast transient response.

The SC419 supports using standard capacitor types such as electrolytic or special polymer in addition to ceramic, at switching frequencies up to 1MHz. The programmable frequency, synchronous operation, and programmable power-save provide high efficiency operation over a wide load range.

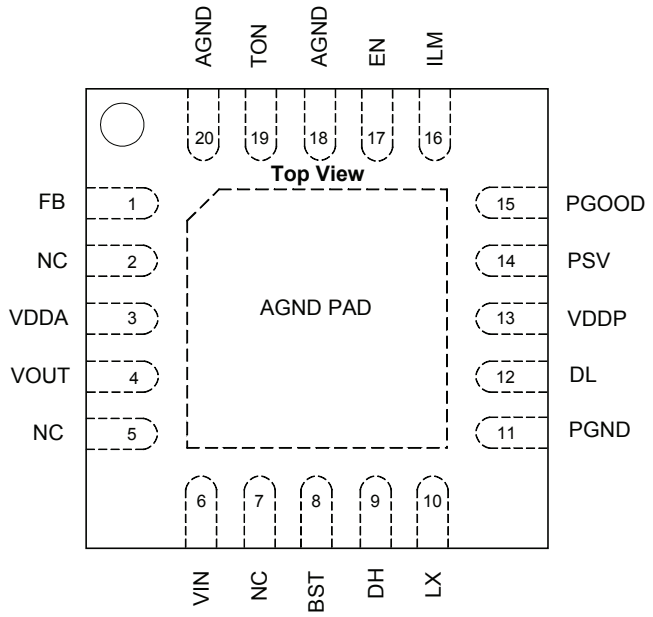
Additional features include cycle-by-cycle current limit, soft-start, under and over-voltage protection, programmable over-current protection, soft shutdown, selectable power-save modes, and programmable ultra-sonic power-save. The device also provides an enable input and a power good output, useful for sequencing multiple devices.

The input voltage can range from 3V to 28V. The wide input voltage range and programmable frequency make the device extremely flexible and easy to use in a broad range of applications. Support is provided for single cell or multi-cell battery systems in addition to traditional DC power supply applications.

Typical Application Circuit



Pin Configuration



MLPQ-UT20

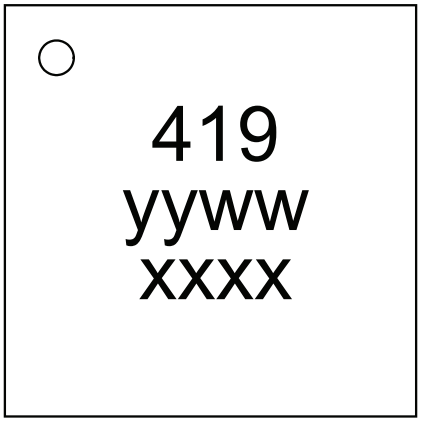
Ordering Information

Device	Package
SC419ULTRT[1)(2)]	MLPQ-UT20
SC419EVB	Evaluation Board

Notes:

1) Available in tape and reel only. A reel contains 3000 devices.
2) Lead-free packaging only. Device is WEEE and RoHS compliant and halogen-free.

Marking Information



yyww = Date Code
xxxx = Semtech Lot Number

Absolute Maximum Ratings[1]

LX to PGND (V) ..... -0.3 to +30
LX to PGND (V) (transient — 100ns) ..... -2 to +30
DH, BST to PGND (V) ..... -0.3 to +35
DH, BST to LX (V) ..... -0.3 to +6
DL to PGND (V) ..... -0.3 to +6
VIN to PGND (V) ..... -0.3 to +30
EN, FB, ILIM, to AGND (V) ..... -0.3 to +(VDDA + 0.3)
PGOOD, PSV, VOUT to AGND (V) .... -0.3 to +(VDDA + 0.3)
TON to AGND (V) ..... -0.3 to +(VDDA -1.5)
VDDP to PGND, VDDA to AGND (V) ..... 0.3 to +6
VDDA to VDDP (V) ..... -0.3 to +0.3
AGND to PGND (V) ..... -0.3 to +0.3

Recommended Operating Conditions

Input Voltage (V) ..... 3.0 to 28
VDDA to AGND (V) ..... 4.5 to 5.5
VDDP to PGND (V) ..... 4.5 to 5.5
VOUT to AGND (V) ..... 0.5 to VDDA

Thermal Information

Storage Temperature (°C) ..... -60 to +150
Maximum Junction Temperature (°C) 150
Operating Junction Temperature (°C) ..... -40 to +125
Thermal resistance, junction to ambient[2] (°C/W) 50
Peak IR Reflow Temperature (°C) 260

Exceeding the above specifications may result in permanent damage to the device or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not recommended.

NOTES:
(1) This device is ESD sensitive. Use of standard ESD handling precautions is required.
(2) Calculated from package in still air, mounted to 3 x 4.5 (in), 4 layer FR4 PCB with thermal vias under the exposed pad per JESD51 standards.

Electrical Characteristics

Unless specified: V_{IN} =12V, VDDA = VDDP = 5V, T_A = +25°C for Typ, -40 to +85 °C for Min and Max, T_J < 125°C, Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Units
Input Supplies					
Input Supply Voltage		3		28	V
VDDA, VDDP Voltage		4.5		5.5	V
VDDA UVLO Threshold	Measured at VDDA pin, rising edge	3.7	3.9	4.1	V
	Measured at VDDA pin, falling edge	3.5	3.6	3.75	
VDDA UVLO Hysteresis			0.3		V
VIN Supply Current	EN = AGND		8.5	20	µA
VDDA + VDDP Supply Current	EN = AGND		3	7	µA
	EN = 5V, R_{PSV} = 115kΩ, V_{FB} > 500mV[1]		3		mA
	EN = 5V, PSV = open (float), V_{FB} > 500mV[1]		0.7		
	Operating f_{SW} = 250kHz, PSV = VDDA, no load[1]		10		
FB On-Time Threshold	Static VIN and load, 0 to +85 °C	0.496	0.500	0.504	V
	Static VIN and load, -40 to +85 °C	0.495		0.505	V

Electrical Characteristics (continued)

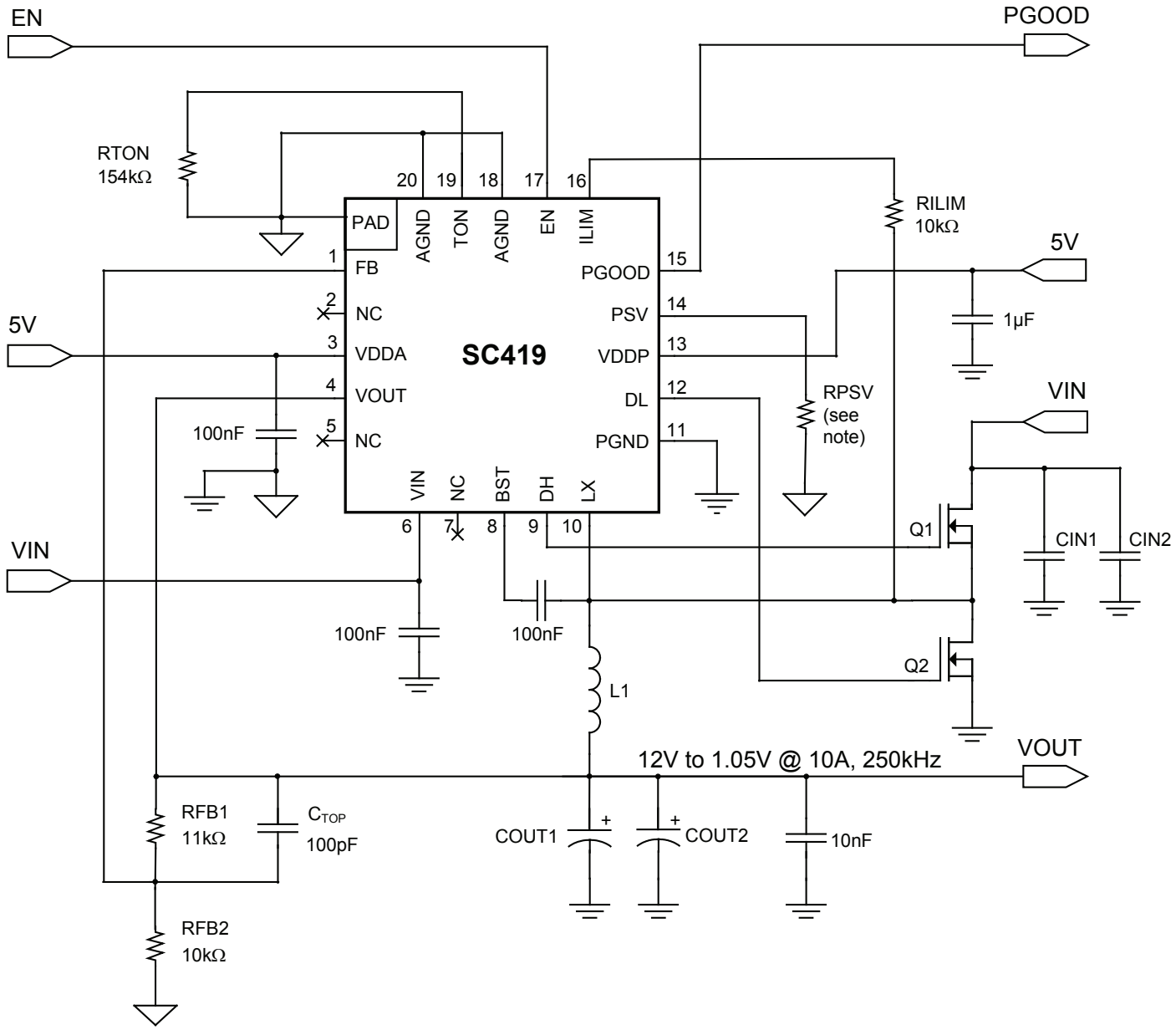
Parameter	Conditions	Min	Typ	Max	Units
Frequency Range	Continuous mode operation			1000	kHz
Timing					
On-Time	Forced continuous mode operation, V_{IN} = 15V, V_{OUT} = 5V, R_{TON} = 300kΩ	2385	2650	2915	ns
Minimum On-Time (1)			80		ns
Minimum Off-Time(1)			250		ns
Soft-Start					
Soft-Start Ramp Time(1)	V_{OUT} ramp from zero to programmed value		850		µs
Analog Inputs/Outputs					
VOUT Input Resistance			500		kΩ
Current Sense					
Zero Cross Detector Threshold	LX - PGND	-7	0	+7	mV
Power Good					
Power Good Threshold	Upper limit, V_{FB} > internal 500mV reference		+20		%
	Lower limit, V_{FB} < internal 500mV reference		-10		%
Start-Up Delay Time	Includes Soft-Start Ramp Time		2		ms
Fault (noise immunity) Delay Time(1)			5		µs
Leakage				1	µA
Power Good On-Resistance			10		Ω
Fault Protection					
I_{LIM} Source Current		9	10	11	µA
I_{LIM} Source Current Temperature Coefficient(1)			0.41		%/°C
I_{LIM} Comparator Offset		-8	0	+8	mV
Output Under-Voltage Threshold	V_{FB} with respect to internal 500mV reference, 8 consecutive cycles		-25		%
Smart Power-Save Protection Threshold(1)	V_{FB} with respect to internal 500mV reference		+10		%
Over-Voltage Protection Threshold	V_{FB} with respect to internal 500mV reference		+20		%
Over-Voltage Fault Delay(1)			5		µs
Over-Temperature Shutdown(1)	10°C hysteresis		150		°C

Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Units
Logic Inputs/Outputs					
Logic Input High Voltage - EN		1.0			V
Logic Input High Voltage - PSV	Forced continuous mode (PSV pulled to VDDA); PSV with respect to VDDA	-0.4			V
Logic Input Low Voltage - EN	With respect to VDDA			0.4	V
EN Input Bias Current	EN = VDDA or AGND	-10		+10	µA
FB Input Bias Current	FB = VDDA or AGND	-1		+1	µA
PSV Input Bias Current	PSV = VDDA		1		µA
High-Side Driver (DH, BST, LX)					
Peak Current[1]			2.0		A
On Resistance	$R_{DH\_PULL-UP}$, LX < 0.5V		3.0	6.0	Ω
	$R_{DH\_PULL-UP}$, LX > 0.5V		1.0	2.0	Ω
	$R_{DH\_PULL-DOWN}$		0.6	1.2	Ω
Rise Time[1]	C_{DH-LX} = 3nF		22		ns
Fall Time[1]	C_{DH-LX} = 3nF		12		ns
Propagation Delay[1]	From FB Comparator Input to DH	30	45	60	ns
Shoot-thru Protection Delay[1]		10	20	30	ns
Bootstrap Switch On Resistance			10		Ω
Low-Side Driver (DL, VDDP, PGND)					
Peak Current[1]			4.0		A
On Resistance	$R_{DL\_PULL-UP}$		1.3	2.1	Ω
	$R_{DL\_PULL-DOWN}$		0.50	0.86	Ω
Rise Time[1]	C_{DL} = 3nF		7		ns
Fall Time[1]	C_{DL} = 3nF		3.5		ns

Notes:
(1) Guaranteed by design.

Detailed Application Circuit



Key Components

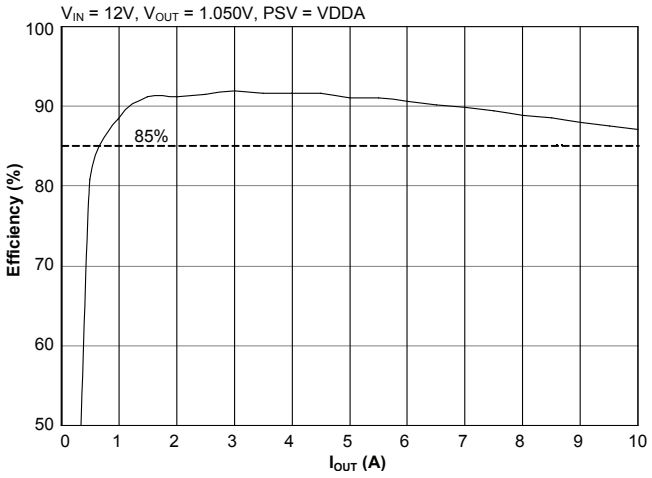
Component	Value	Manufacturer	Part Number	Web
CIN1, CIN2	10µF/25V	Murata	GRM32DR71E106KA12L	www.murata.com
COUT1, COUT2	220µF/15mΩ/6.3V	Panasonic	EEFUE0J221R	www.panasonic.com
L1 (option 1)	0.88µH/2.3mΩ	NEC-Tokin	MPC1040LR88C	www.nec-tokin.co
L1 (option 2)	1.0µH/2.3mΩ	Vishay	IHLP4040DZER1R0M11	www.vishay.co
Q1	IRF7821	I.R.	IRF7821	www.irf.com
Q2	IRF7832	I.R.	IRF7832	www.irf.com

Note - RPSV: Use 115kΩ for Ultrasonic operation
Remove RPSV for Power-Save operation
Connect PSV pin to VDDA for Forced Continuous Mode operation

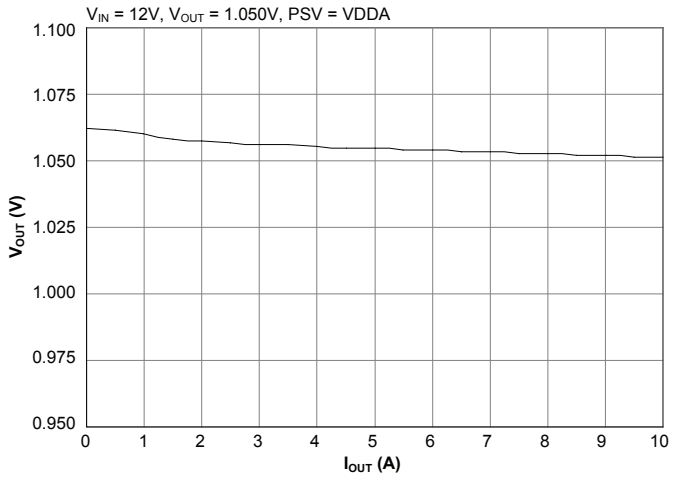
Typical Characteristics

Characteristics in this section are based on using the Detailed Application Circuit.

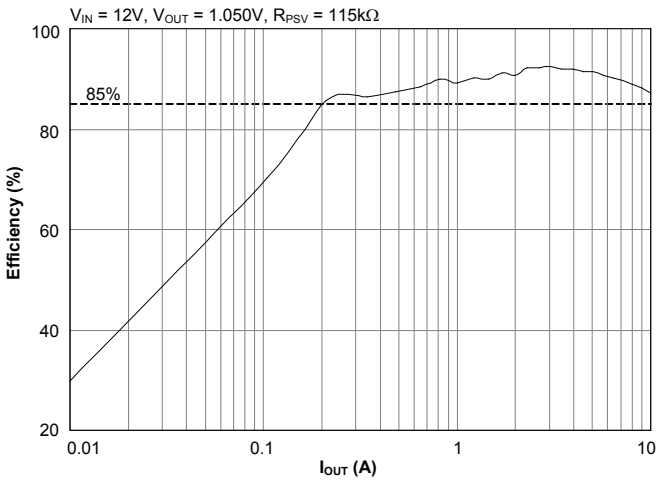
Efficiency vs. Load — Forced Continuous Mode



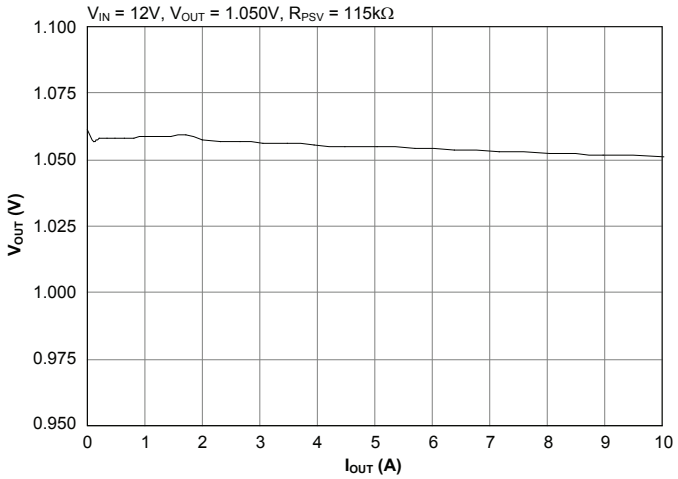
V_{OUT} vs. Load — Forced Continuous Mode



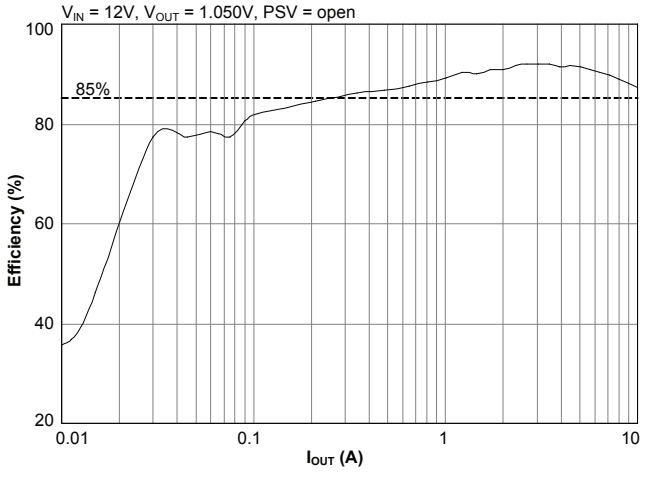
Efficiency vs. Load — Ultrasonic Power-save



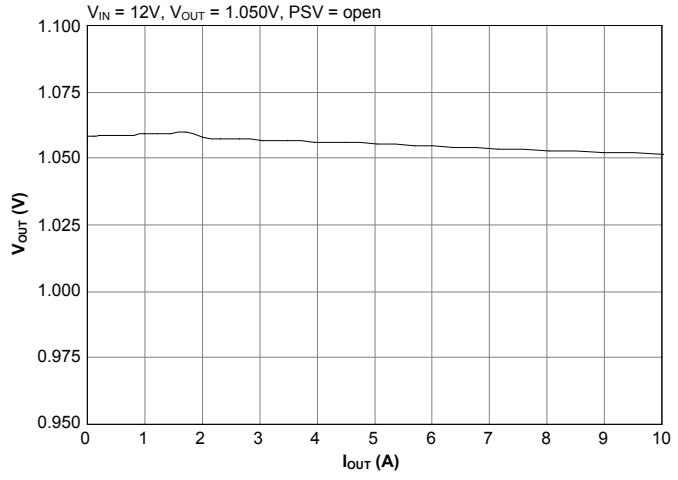
V_{OUT} vs. Load — Ultrasonic Power-save Mode



Efficiency vs. Load — Power-save Mode



V_{OUT} vs. Load — Power-save Mode

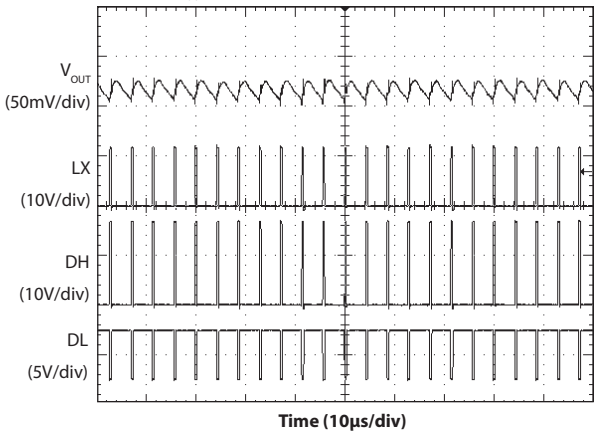


Typical Characteristics (continued)

Characteristics in this section are based on using the Detailed Application Circuit.

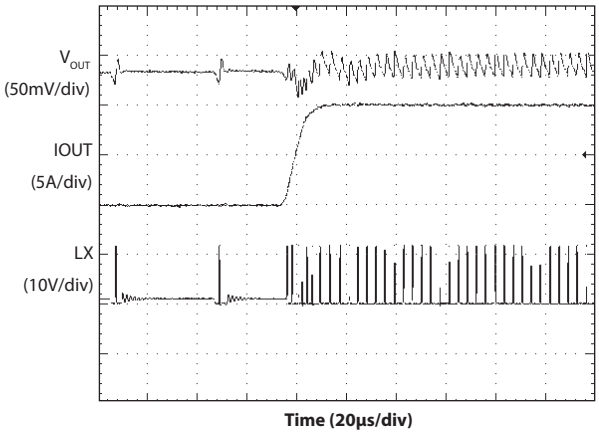
Forced Continuous Operation — No Load

V_{IN} = 12V, V_{OUT} = 1.05V, PSV = VDDA



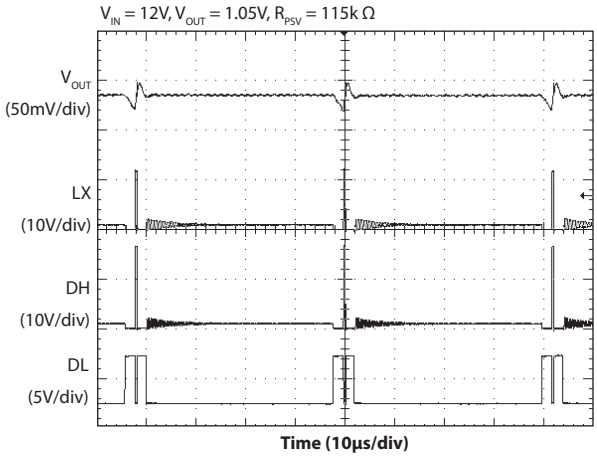
Transient Response — Load Rising

V_{IN} = 12V, V_{OUT} = 1.05V, R_{PSV} = 115k Ω, I_{OUT} = 0A to 10A



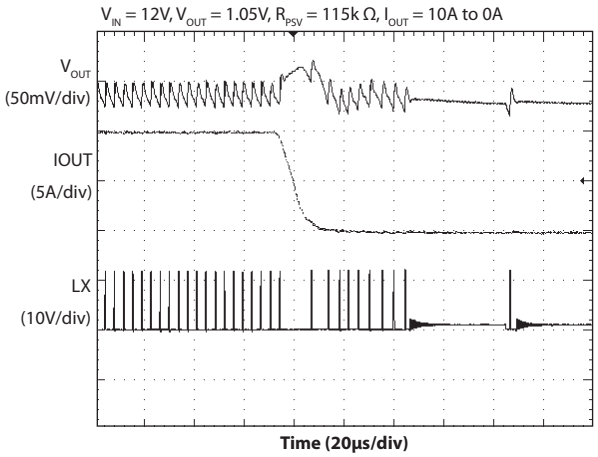
Ultrasonic Power-save Operation — No Load

V_{IN} = 12V, V_{OUT} = 1.05V, R_{PSV} = 115k Ω



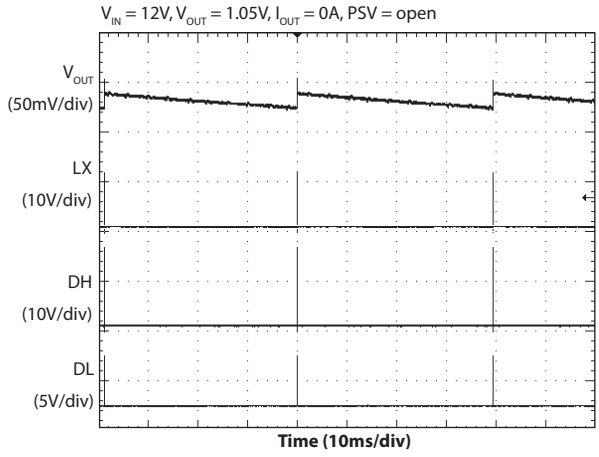
Transient Response — Load Falling

V_{IN} = 12V, V_{OUT} = 1.05V, R_{PSV} = 115k Ω, I_{OUT} = 10A to 0A



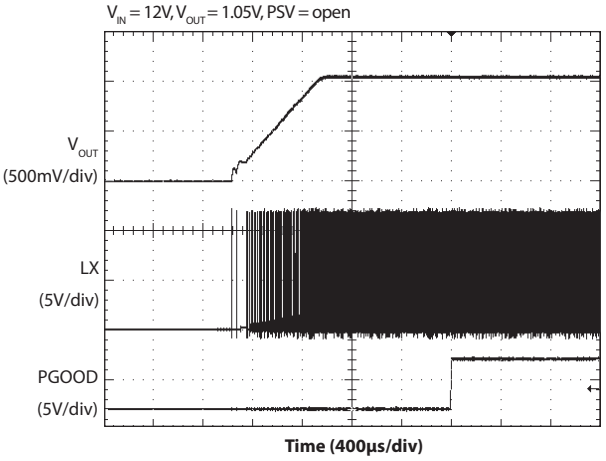
Power-save Operation — No Load

V_{IN} = 12V, V_{OUT} = 1.05V, I_{OUT} = 0A, PSV = open



Enable to Power Good True

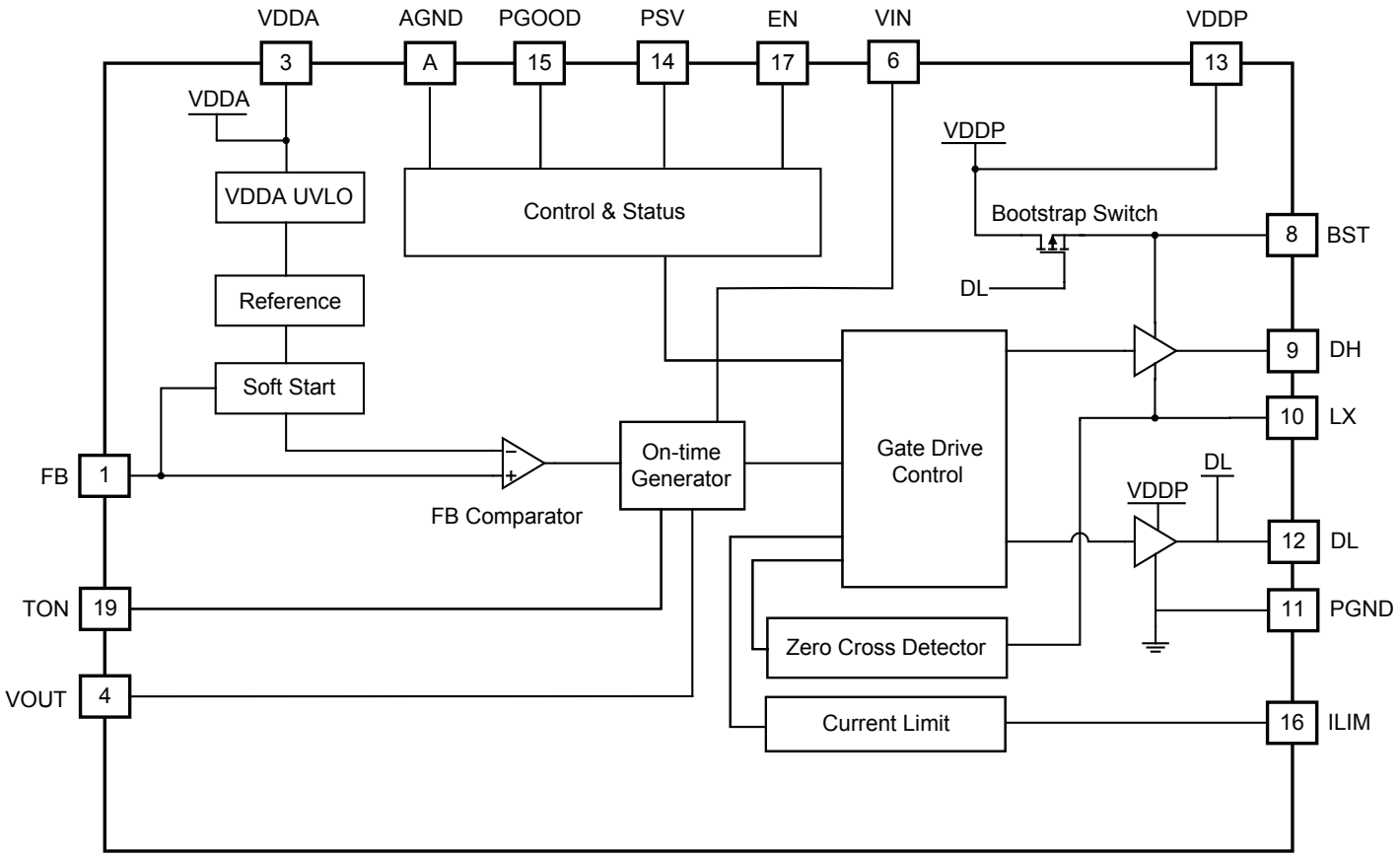
V_{IN} = 12V, V_{OUT} = 1.05V, PSV = open



Pin Descriptions

Pin #	Pin Name	Pin Function
1	FB	Feedback input for switching regulator — connect to an external resistor divider from output — used to program the output voltage.
2	NC	No Connection
3	VDDA	Supply input for internal analog circuits — connect to 5V supply — and the sense input for VDDA UVLO. Bypass with a 100nF minimum capacitor to AGND.
4	VOUT	Output voltage sense pin
5	NC	No Connection
6	VIN	Input supply voltage — connect to the same supply as the high-side MOSFET. Connect a 100nF capacitor to AGND.
7	NC	No Connection
8	BST	Bootstrap pin — connect a 100nF minimum capacitor from BST to LX to develop the floating voltage for the high-side gate drive.
9	DH	High-side gate drive output
10	LX	Switching (phase) node
11	PGND	Power ground
12	DL	Low-side gate drive output
13	VDDP	Supply input for the DH and DL gate drives — connect to the same 5V supply used for VDDA. Bypass with a 1µF minimum capacitor to PGND.
14	PSV	Power-save programming input — connect a resistor to AGND to set the minimum power-save frequency. Float pin to select power-save at no minimum frequency or pull up to VDDA to disable power-save.
15	PGOOD	Open-drain Power Good indicator — high impedance indicates the switching regulator output power is good. An external pull-up resistor is required.
16	ILIM	Current limit sense pin — used to program the current limit by connecting a resistor from ILIM to LX.
17	EN	Enable input for switching regulator — logic low disables the switching regulator or logic high enables the switching regulator.
18	AGND	Analog ground
19	TON	ON time programming input — set the on-time by connecting through a resistor to AGND.
20	AGND	Connect this pin to AGND along with pins 18 and PAD.
PAD	AGND	Analog ground

Block Diagram



A = connected to pins 18, 20, and PAD

Not used: pins 2, 5, 7

Applications Information

General Description

The SC419 is a step down synchronous DC-DC buck controller. It provides high efficiency operation in a space saving 3 x 3 (mm) 20-pin package. The programmable operating frequency range from 200kHz to 1MHz enables optimizing the configuration for PCB area and efficiency.

The controller uses a pseudo-fixed frequency adaptive on-time control. This allows fast transient response which permits the use of smaller output capacitors.

Input Voltage Requirements

The SC419 requires three input supplies for normal operation: V_{IN}, VDDA, and VDDP. V_{IN} can operate over the wide range of 3V to 28V. VDDA and VDDP require an external 5V supply. VDDA and VDDP should be connected to the same source voltage.

Psuedo-fixed Frequency Adaptive On-time Control

The PWM control method used by the SC419 is pseudo-fixed frequency, adaptive on-time, as shown in Figure 1. The ripple voltage generated at the output capacitor ESR is used as a PWM ramp signal. This ripple is used to trigger the on-time of the controller.

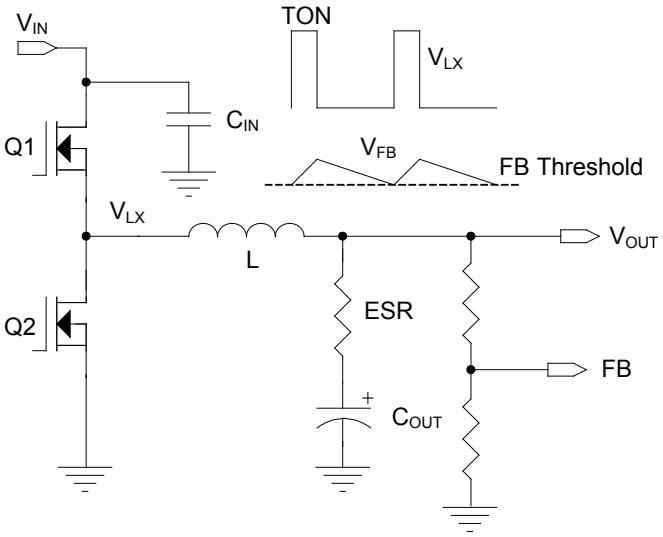


Figure 1 — PWM Control Method, V_{OUT} Ripple

The adaptive on-time is determined by an internal one-shot timer. When the one-shot is triggered by the output ripple, the device sends a single on-time pulse to the high-side MOSFET. The pulse period is determined by V_{OUT} and V_{IN}. The period is proportional to output voltage and inversely proportional to input voltage. With this adaptive on-time configuration, the device automatically anticipates the on-time needed to regulate V_{OUT} for the present V_{IN} condition and at the selected frequency.

The advantages of adaptive on-time control are:

- Predictable operating frequency compared to other variable frequency methods.
- Reduced component count by eliminating the error amplifier and compensation components.
- Reduced component count by removing the need to sense and control inductor current.
- Fast transient response — the response time is controlled by a fast comparator instead of a typically slow error amplifier.
- Reduced output capacitance due to fast transient response.

One-Shot Timer and Operating Frequency

One-shot timer operation is shown in Figure 2. The FB comparator output goes high when V_{FB} is less than the internal 500mV reference. This feeds into the gate drive and turns on the high-side MOSFET, and also starts the one-shot timer. The one-shot timer uses an internal comparator and a capacitor. One comparator input is connected to V_{OUT}, the other input is connected to the capacitor. When the on-time begins, the internal capacitor charges from zero volts through a current which is proportional to V_{IN}. When the capacitor voltage reaches V_{OUT}, the on-time is completed and the high-side MOSFET turns off.

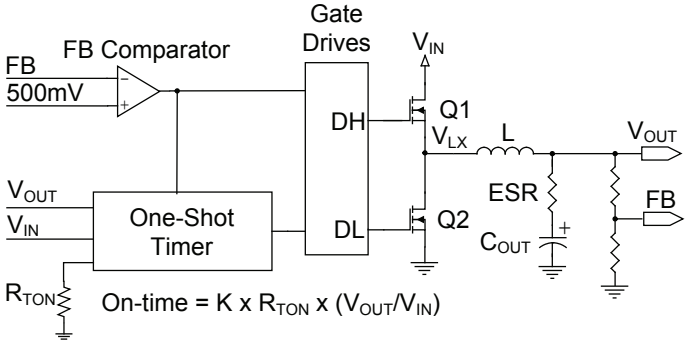


Figure 2 — On-Time Generation

Applications Information (continued)

This method automatically produces an on-time that is proportional to V_{OUT} and inversely proportional to V_{IN}. Under steady-state conditions, the switching frequency can be determined from the on-time by the following equation.

$$f_{SW} = \frac{V_{OUT}}{T_{ON} \times V_{IN}}$$

The SC419 uses an external resistor to set the on-time which indirectly sets the frequency. The on-time can be programmed to provide an operating frequency from 200kHz to 1MHz using a resistor between the TON pin and ground. The resistor value is selected by the following equation.

$$R_{TON} = \frac{(T_{ON} - 10ns) \times V_{IN}}{25pF \times V_{OUT}}$$

The maximum R_{TON} value allowed is shown by the following equation.

$$R_{TON\_MAX} = \frac{V_{IN\_MIN}}{15\mu A}$$

Immediately after the on-time, the DL output drives high to energize the low-side MOSFET. DL has a minimum high time of ~250ns, after which DL continues to stay high until one of the following occurs:

- VFB falls below the 500mV reference
- The Zero Cross Detector trips if power-save is active

V_{OUT} Voltage Selection

The output voltage is regulated by comparing V_{OUT} as seen through a resistor divider at the FB pin to the internal 500mV reference (see Figure 3).

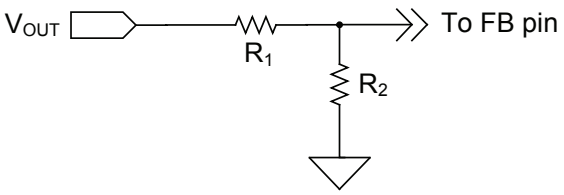


Figure 3 — Output Voltage Selection

Note that this control method regulates the valley of the output ripple voltage, not the DC value. The DC value of V_{OUT} is offset by the output ripple according to the following equation.

$$V_{OUT} = 0.5 \times \left(1 + \frac{R_1}{R_2}\right) + \left(\frac{V_{RIPPLE}}{2}\right)$$

Forced Continuous Mode Operation

The SC419 operates in FCM (Forced Continuous Mode) by connecting the PSV pin to VDDA. (The PSV pin should not exceed the VDDA supply.) See Figure 4 for FCM waveforms. In this mode one of the power MOSFETs is always on, with no intentional dead time other than to avoid cross-conduction. This results in uniform frequency across the full load range with the trade-off being reduced efficiency at light loads due to the high-frequency switching of the MOSFETs.

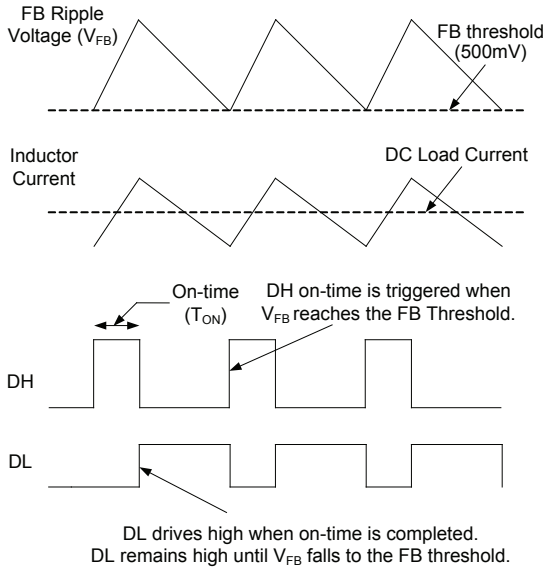


Figure 4 — Forced Continuous Mode Operation

The switcher output voltage can be programmed higher than 5V with careful design. In this case the VOUT pin cannot connect directly to the switcher output due to its the maximum voltage rating. An additional resistor divider network is required to connect from the switcher output to the VOUT pin. The voltage at the VOUT pin should be at least 500mV lower than the VDDA supply, to prevent the VLDO switch-over function. For example, the voltage at the VOUT pin can be 4V if VDDA is set for 5V. When the SC418 operates from an external power source and the LDO is disabled by grounding the ENL pin, the voltage at the VOUT pin can be as high as shown in Recommended Operating Conditions. Note that RTON must be adjusted higher by the same divider ratio to

Applications Information (continued)

maintain the desired on-time. On-time is calculated according to the voltage at the VOUT pin.

Programmable Ultra-sonic Power-Save Operation

The device provides programmable ultra-sonic power-save operation at light loads. The minimum operating frequency is programmed by connecting a resistor from PSV to AGND. The SC419 uses the PSV resistor to set an internal timer that monitors the time between consecutive high-side gate pulses. If the time exceeds the programmed timer, DL drives high to turn the low-side MOSFET on. This draws current from V_{OUT} through the inductor, forcing both V_{OUT} and V_{FB} to fall. When V_{FB} drops to the 500mV threshold, the next DH on-time is triggered. After the on-time is completed the high-side MOSFET is turned off and the low-side MOSFET turns on, and the internal timer is restarted. The low-side MOSFET remains on until the inductor current ramps down to zero, at which point the low-side MOSFET is turned off. This ends the cycle until V_{FB} falls below the 500mV threshold, or the internal timer forces another DL turn-on.

Because the period between on-times is limited to a maximum value, a minimum operating frequency is maintained. Figure 5 shows ultrasonic power-save operation.

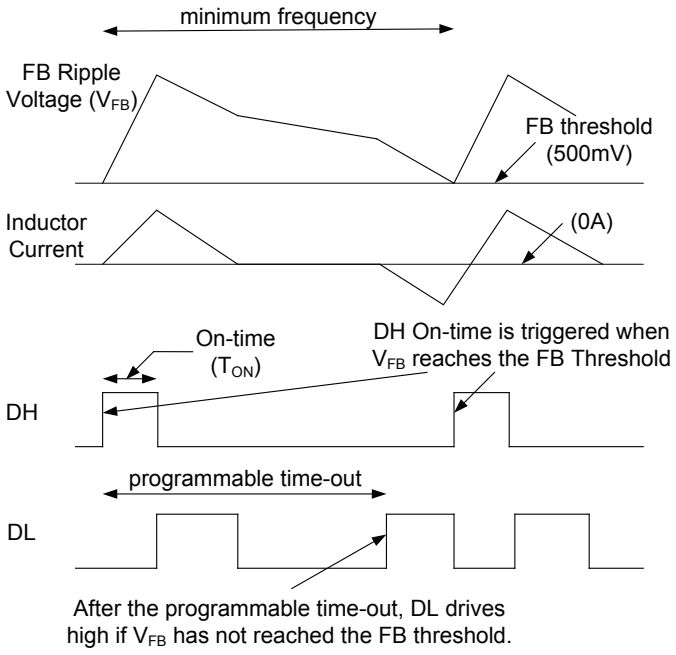


Figure 5 — Ultrasonic Power-Save Operation

The equation for determining the R_{PSV} resistor value is shown next. The desired minimum frequency is f_{SWMIN}.

$$R_{PSV} = \frac{1}{350pF \times f_{SWMIN}}$$

Power-Save Mode Operation

The device provides power-save operation at light loads with no minimum operating frequency, selected by floating the PSV pin (no connection). In this mode of operation, the internal zero crossing comparator monitors the inductor current via the voltage across the low-side MOSFET during the off-time. If the inductor current falls to zero for 8 consecutive switching cycles, the controller enters power-save operation. It will then turn off the low-side MOSFET on each subsequent cycle, provided that the current crosses zero. After the low-side MOSFET is off, both high-side and low-sides MOSFETs remain off until V_{FB} drops to the 500mV threshold. While the MOSFETs are off the load is supplied by the output capacitor. If the inductor current does not reach zero on any switching cycle, the controller immediately exits power-save and returns to forced continuous mode. Figure 6 shows power-save operation at light loads.

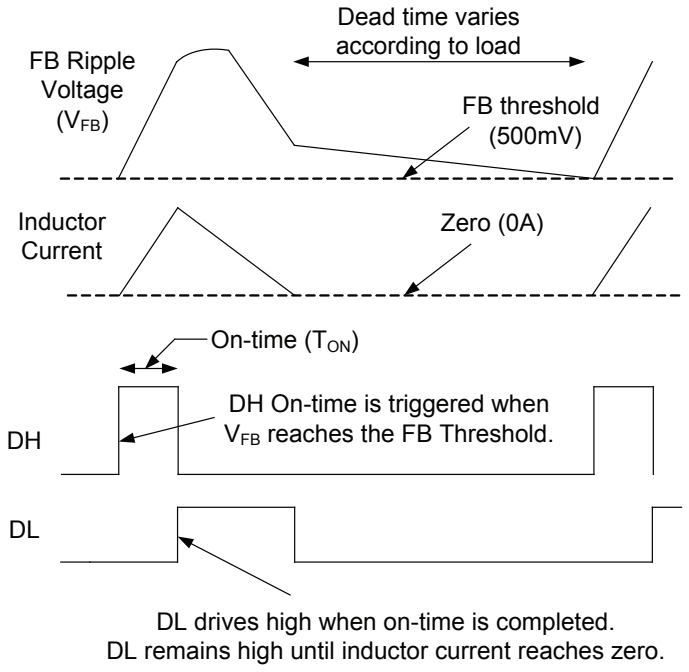


Figure 6 — Power-Save Operation

Applications Information (continued)

Smart Power-Save Protection

Active loads may leak current from a higher voltage into the output. Under light load conditions with power-save enabled, this can force V_{OUT} to slowly rise and reach the over-voltage threshold, resulting in a hard shutdown. Smart power-save prevents this condition. When the FB voltage exceeds 10% above nominal (exceeds 550mV), the device immediately disables power-save and DL drives high to turn on the low-side MOSFET. This draws current from V_{OUT} through the inductor and causes V_{OUT} to fall. When V_{FB} drops back to the 500mV trip point, a normal T_{ON} switching cycle begins. This method prevents a hard OVP shutdown and cycles energy from V_{OUT} back to V_{IN}. It also minimizes operating power by avoiding forced conduction mode operation. Figure 7 shows typical waveforms for the Smart Power-save feature.

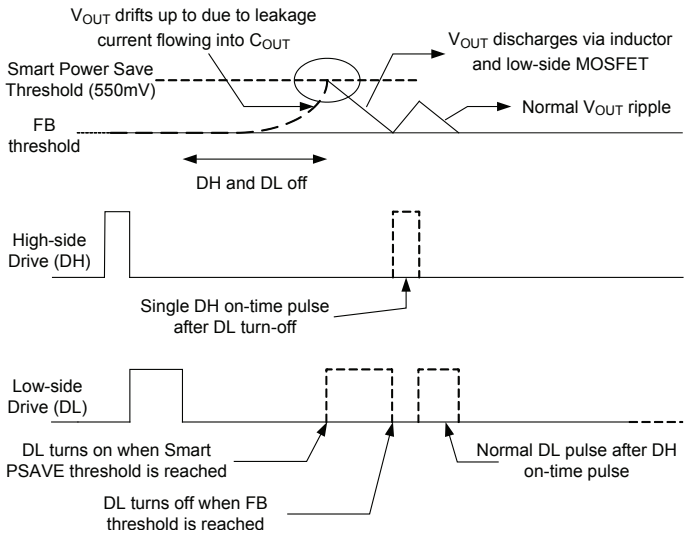


Figure 7 — Smart Power-Save

Enable Input

The EN input is a logic level input. When EN is low (grounded), the regulator is off and in its lowest power state. When EN is low and VDDA is above the VDDA UVLO threshold, the output soft-discharges into the V_{OUT} pin through an internal 15Ω resistor. When EN is a logic high (≥1V) the switching regulator is enabled.

The EN input has internal resistors: a 2MΩ pullup to VDDA, and a 1MΩ pulldown to AGND. These resistors will normally cause the EN voltage to be above the logic high trip point as VDDA reaches the VDDA UVLO threshold. To prevent undesired or erratic startup, the EN pin should not be allowed to float as open-circuit.

Current Limit Protection

The SC419 features programmable current limiting, which is accomplished using the RDSON of the lower MOSFET for current sensing. The current limit is set by R_{ILIM} resistor which connects from the ILIM pin to the drain of the low-side MOSFET. When the low-side MOSFET is on, an internal 10µA current flows from the ILIM pin and through the R_{ILIM} resistor, creating a voltage drop across the resistor. While the low-side MOSFET is on, the inductor current flows through it and creates a voltage across the $RDS_{(ON)}$. The voltage across the MOSFET is negative with respect to PGND. If this MOSFET voltage drop exceeds the voltage across R_{ILIM}, the voltage at the ILIM pin will be negative and current limit will activate. The current limit then keeps the low-side MOSFET on, preventing another high-side on-time until the current in the low-side MOSFET reduces enough to bring the voltage at the ILIM pin back up to zero. This method regulates the inductor valley current at the level shown by I_{LIM} in Figure 8.

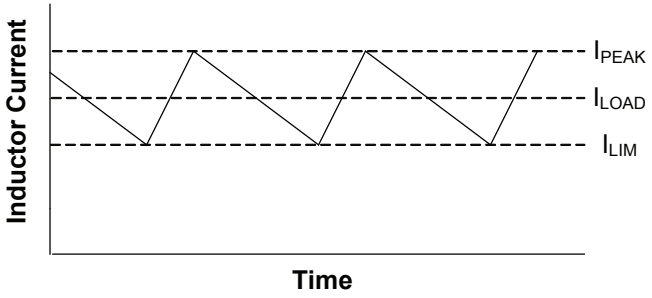


Figure 8 — Valley Current Limit

Applications Information (continued)

The current limit schematic with the R_{ILIM} resistor is shown in Figure 9.

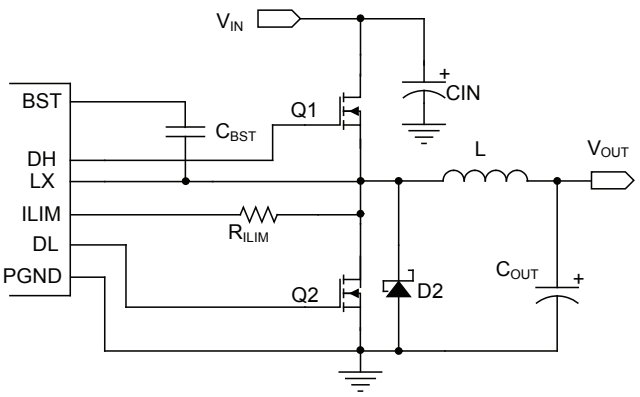


Figure 9 — Valley Current Limit

Setting the valley current limit to 10A results in a peak inductor current of 10A plus peak ripple current. In this situation the average current through the inductor is 10A plus one-half the peak-to-peak ripple current.

The R_{ILIM} value is calculated by the next equation.

$$R_{ILIM} = \frac{R_{DSON} \times I_{LIM}}{10\mu A}$$

Soft-Start of PWM Regulator

Soft-start is achieved in the PWM regulator by using an internal voltage ramp as the reference for the FB comparator. The voltage ramp is generated using an internal charge pump which drives the reference from zero to 500mV in 1.2mV increments, using an internal 500kHz oscillator. When the ramp voltage reaches 500mV, the ramp is ignored and the FB comparator switches over to a fixed 500mV threshold. During soft-start the output voltage tracks the internal ramp, which limits the start-up inrush current and provides a controlled soft-start profile. Typical soft-start ramp time is 850µs.

During soft-start the regulator turns off the low-side MOSFET on any cycle if the inductor current falls to zero, regardless of the PSAVE mode setting. This prevents negative inductor current, allowing the device to start into a pre-biased output.

Power Good Output

The PGOOD (Power Good) output is an open-drain output which requires a pull-up resistor. When the voltage at the FB pin is 10% below the nominal voltage, PGOOD is pulled low. It is held low until the FB voltage returns above -8% of nominal. PGOOD is held low during start-up and will not be allowed to transition high until soft-start is completed (when V_{FB} reaches 500mV). The delay time starting from EN going high is typically 2ms.

PGOOD will transition low if the FB voltage exceeds +20% of nominal, which is also the over-voltage threshold (600mV). PGOOD also pulls low if the EN pin is low when VDDA is present.

Output Over-Voltage Protection

OVP (Over-voltage protection) becomes active as soon as the device is enabled. The OVP threshold is set at 500mV + 20% (600mV). When V_{FB} exceeds the OVP threshold, DL latches high and the low-side MOSFET is turned on. DL remains high and the controller remains off until the EN input is toggled or VDDA is cycled. There is a 5µs delay built into the OVP detector to prevent false transitions. PGOOD is also low after an OVP event.

Output Under-Voltage Protection

When V_{FB} falls 25% below its nominal voltage (falls to 375mV) for eight consecutive clock cycles, the switcher is shut off and the DH and DL drives are pulled low to tri-state the MOSFETs. The controller stays off until EN is toggled or VDDA is cycled.

VDDA UVLO and POR

The VDDA Under-Voltage Lock-Out (UVLO) circuitry inhibits switching and tri-states the DH/DL drivers until VDDA rises above 3.9V. When VDDA exceeds 3.9V, an internal POR (Power-On Rese) resets the fault latch and the soft-start counter and then the SC419 begins the soft-start cycle. The device will shut off if VDDA falls below 3.6V. VDDP does not have ULVO protection.

SEMTECH

Applications Information (continued)

Design Procedure

When designing a switch mode supply the input voltage range, load current, switching frequency, and inductor ripple current must be specified.

The maximum input voltage (V_{INMAX}) is the highest specified input voltage. The minimum input voltage (V_{INMIN}) is determined by the lowest input voltage after evaluating the voltage drops due to connectors, fuses, switches, and PCB traces.

The following parameters define the design.

- Nominal output voltage (V_{OUT})
- Static or DC output tolerance
- Transient response
- Maximum load current (I_{OUT})

There are two values of load current to evaluate — continuous load current and peak load current. Continuous load current relates to thermal stresses which drive the selection of the inductor and input capacitors. Peak load current determines instantaneous component stresses and filtering requirements such as inductor saturation, output capacitors, and design of the current limit circuit.

The following values are used in this design.

- V_{IN} = 12V ± 10%
- V_{OUT} = 1.05V ± 4%
- f_{SW} = 250kHz
- Load = 10A maximum

Frequency Selection

Selection of the switching frequency requires making a trade-off between the size and cost of the external filter components (inductor and output capacitor) and the power conversion efficiency.

The desired switching frequency is 250kHz.

A resistor, R_{TON} is used to program the on-time (indirectly setting the frequency) using the following equation.

$$R_{TON} = \frac{(T_{ON} - 10ns) \times V_{IN}}{25pF \times V_{OUT}}$$

To select R_{TON}, use the maximum value for V_{IN}, and for T_{ON} use the value associated with maximum V_{IN}.

$$T_{ON} = \frac{V_{OUT}}{V_{INMAX} \times f_{SW}}$$

T_{ON} = 318 ns at 13.2V_{IN}, 1.05V_{OUT}, 250kHz

Substituting for R_{TON} results in the following solution.

R_{TON} = 154.9kΩ, use R_{TON} = 154kΩ

Inductor Selection

In order to determine the inductance, the ripple current must first be defined. Low inductor values result in smaller size but create higher ripple current which can reduce efficiency. Higher inductor values will reduce the ripple current/voltage and for a given DC resistance are more efficient. However, larger inductance translates directly into larger packages and higher cost. Cost, size, output ripple, and efficiency are all used in the selection process.

The ripple current will also set the boundary for power-save operation. The switching will typically enter power-save mode when the load current decreases to 1/2 of the ripple current. For example, if ripple current is 4A then Power-save operation will typically start for loads less than 2A. If ripple current is set at 40% of maximum load current, then power-save will start for loads less than 20% of maximum current.

The inductor value is typically selected to provide a ripple current that is between 25% to 50% of the maximum load current. This provides an optimal trade-off between cost, efficiency, and transient performance.

During the DH on-time, voltage across the inductor is (V_{IN} - V_{OUT}). The following equation is used to determine the inductance.

$$L = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{I_{RIPPLE}}$$

In this example the inductor ripple current is set equal to 50% of the maximum load current. Thus ripple current will be 50% x 10A or 5A.

Applications Information (continued)

To find the minimum inductance needed, use the V_{IN} and T_{ON} values that correspond to V_{INMAX}.

$$L = \frac{(13.2 - 1.05) \times 318ns}{5A} = 0.77\mu H$$

A slightly larger value of 0.88µH is selected. This will decrease the maximum I_{RIPPLE} to 4.4A.

Note that the inductor must be rated for the maximum DC load current plus 1/2 of the ripple current.

The ripple current under minimum V_{IN} conditions is also checked using the following equations.

$$T_{ON\_VINMIN} = \frac{25pF \times R_{TON} \times V_{OUT}}{V_{INMIN}} + 10ns = 384ns$$

$$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{L}$$

$$I_{RIPPLE\_VINMIN} = \frac{(10.8 - 1.05) \times 384ns}{088\mu H} = 4.25A$$

Capacitor Selection

The output capacitors are chosen based on required ESR and capacitance. The maximum ESR requirement is controlled by the output ripple requirement and the DC tolerance. The output voltage has a DC value that is equal to the valley of the output ripple plus 1/2 of the peak-to-peak ripple. Change in the output ripple voltage will lead to a change in DC voltage at the output.

The design goal is for the output voltage regulation to be ±4% under static conditions. The internal 500mV reference tolerance is 1%. Allowing 1% tolerance from the FB resistor divider, this allows 2% tolerance due to V_{OUT} ripple. Since this 2% error comes from 1/2 of the ripple voltage, the allowable ripple is 4%, or 42mV for a 1.05V output.

The maximum ripple current of 4.4A creates a ripple voltage across the ESR. The maximum ESR value allowed is shown by the following equations.

$$ESR_{MAX} = \frac{V_{RIPPLE}}{I_{RIPPLEMAX}} = \frac{42mV}{4.4A}$$

$$ESR_{MAX} = 9.5\ m\Omega$$

The output capacitance is chosen to meet transient requirements. A worst-case load release, from maximum load to no load at the exact moment when inductor current is at the peak, determines the required capacitance. If the load release is instantaneous (load changes from maximum to zero in < 1µs), the output capacitor must absorb all the inductor's stored energy. This will cause a peak voltage on the capacitor according to the following equation.

$$COUT_{MIN} = \frac{L\left(I_{OUT} + \frac{1}{2} \times I_{RIPPLEMAX}\right)^2}{(V_{PEAK})^2 - (V_{OUT})^2}$$

Assuming a peak voltage V_{PEAK} of 1.150 (100mV rise upon load release), and a 10A load release, the required capacitance is shown by the next equation.

$$COUT_{MIN} = \frac{0.88\mu H\left(10 + \frac{1}{2} \times 4.4\right)^2}{(1.15)^2 - (1.05)^2}$$

$$COUT_{MIN} = 595\mu F$$

If the load release is relatively slow, the output capacitance can be reduced. At heavy loads during normal switching, when the FB pin is above the 500mV reference, the DL output is high and the low-side MOSFET is on. During this time, the voltage across the inductor is approximately $-V_{OUT}$. This causes a down-slope or falling di/dt in the inductor. If the load di/dt is not faster than the -di/dt in the inductor, then the inductor current will tend to track the falling load current. This will reduce the excess inductive energy that must be absorbed by the output capacitor, therefore a smaller capacitance can be used.

The following five equations can be used to calculate the needed capacitance for a given dI_{LOAD}/dt.

Peak inductor current is shown by the next equation.

$$I_{LPK} = I_{MAX} + 1/2 \times I_{RIPPLEMAX}$$

$$I_{LPK} = 10 + 1/2 \times 4.4 = 12.2A$$

$$\text{Rate of change of Load Current} = \frac{dI_{LOAD}}{dt}$$

Applications Information (continued)

I_{MAX} = maximum load release = 10A

$$C_{OUT} = I_{LPK} \times \frac{L \times \frac{I_{LPK}}{V_{OUT}} - \frac{I_{MAX}}{dI_{LOAD}} \times dt}{2(V_{PK} - V_{OUT})}$$

Example

$$\frac{dI_{LOAD}}{dt} = \frac{2.5A}{\mu s}$$

This would cause the output current to move from 10A to zero in 4µs. The output capacitance required in this case is shown by the following equation.

$$C_{OUT} = 12.2 \times \frac{0.88\mu H \times \frac{12.2}{1.05} - \frac{10}{2.5} \times 1\mu s}{2(1.15 - 1.05)}$$

$$C_{OUT} = 379\ \mu F$$

Note that C_{OUT} is much smaller in this example, 379µF compared to 595µF based on a worst-case load release. To meet the two design criteria of minimum 379µF and maximum 9mΩ ESR, select two capacitors rated at 220µF and 15mΩ ESR.

It is recommended that an additional small capacitor be placed in parallel with C_{OUT} in order to filter high frequency switching noise.

Stability Considerations

Unstable operation is possible with adaptive on-time controllers, and usually takes the form of double-pulsing or ESR loop instability.

Double-pulsing occurs due to switching noise seen at the FB input or because the FB ripple voltage is too low. This causes the FB comparator to trigger prematurely after the 250ns minimum off-time has expired. In extreme cases the noise can cause three or more successive on-times. Double-pulsing will result in higher ripple voltage at the output, but in most applications it will not affect operation. This form of instability can usually be avoided by providing the FB pin with a smooth, clean ripple signal that is at least 10mVp-p, which may dictate the need to increase the ESR of the output capacitors. It is also imperative to provide a proper PCB layout as discussed in the Layout Guidelines section.

Another way to eliminate doubling-pulsing is to add a small capacitor across the upper feedback resistor, as shown in Figure 10. This capacitor should be left unpopulated unless it can be confirmed that double-pulsing exists. Adding the C_{TOP} capacitor will couple more ripple into FB to help eliminate the problem. An optional connection on the PCB should be available for this capacitor.

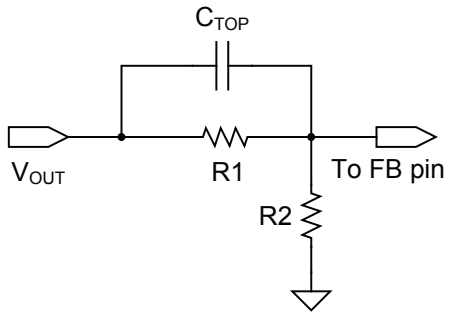


Figure 10 — Capacitor Coupling to FB Pin

ESR loop instability is caused by insufficient ESR. The details of this stability issue are discussed in the ESR Requirements section. The best method for checking stability is to apply a zero-to-full load transient and observe the output voltage ripple envelope for overshoot and ringing. Ringing for more than one cycle after the initial step is an indication that the ESR should be increased.

One simple way to solve this problem is to add trace resistance in the high current output path. A side effect of adding trace resistance is decreased load regulation.

ESR Requirements

A minimum ESR is required for two reasons. One reason is to generate enough output ripple voltage to provide 10mVp-p at the FB pin (after the resistor divider) to avoid double-pulsing.

The second reason is to prevent instability due to insufficient ESR. The on-time control regulates the valley of the output ripple voltage. This ripple voltage is the sum of the two voltages. One is the ripple generated by the ESR, the other is the ripple due to capacitive charging and dis-

Applications Information (continued)

charging during the switching cycle. For most applications the ripple voltage is dominated by the ESR of the output capacitors, typically SP or POSCAP devices. For stability the ESR zero of the output capacitor should be lower than approximately one-third the switching frequency. The formula for minimum ESR is shown by the following equation.

$$ESR_{MIN} = \frac{3}{2 \times \pi \times C_{OUT} \times f_{sw}}$$

When applications use ceramic output capacitors, the ESR is normally too small to meet the minimum ESR criteria. In these applications it is necessary to add a small virtual ESR network composed of two capacitors and one resistor, as shown in Figure 11. This network creates a ramp voltage across C_L, analogous to the ramp voltage generated across the ESR of a standard capacitor. This ramp is then capacitively coupled into the FB pin via capacitor C_C.

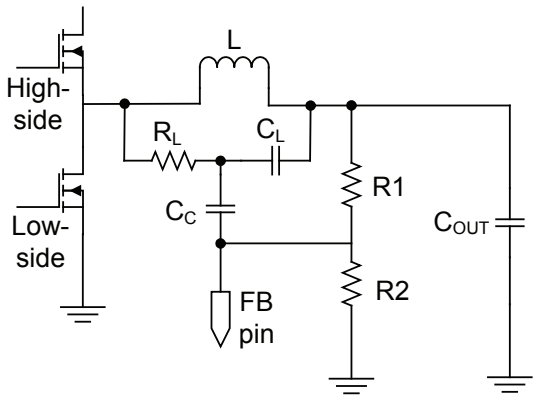


Figure 11 — Virtual ESR Ramp Current

Dropout Performance

The output voltage adjust range for continuous-conduction operation is limited by the fixed 250ns (typical) minimum off-time of the one-shot. When working with low input voltages, the duty-factor limit must be calculated using worst-case values for on and off times.

The duty-factor limitation is shown by the following equation.

$$DUTY = \frac{T_{ON(MIN)}}{T_{ON(MIN)} + T_{OFF(MAX)}}$$

The inductor resistance and MOSFET on-state voltage drops must be included when performing worst-case dropout duty-factor calculations.

System DC Accuracy

Three factors affect V_{OUT} accuracy: the trip point of the FB error comparator, the ripple voltage variation with line and load, and the external resistor tolerance. The error comparator offset is trimmed so that under static conditions it trips when the feedback pin is 500mV, 1%.

The on-time pulse from the SC419 in the design example is calculated to give a pseudo-fixed frequency of 250kHz. Some frequency variation with line and load is expected. This variation changes the output ripple voltage. Because adaptive on-time converters regulate to the valley of the output ripple, ½ of the output ripple appears as a DC regulation error. For example, if the output ripple is 50mV with V_{IN} = 6 volts, then the measured DC output will be 25mV above the comparator trip point. If the ripple increases to 80mV with V_{IN} = 25V, then the measured DC output will be 40mV above the comparator trip. The best way to minimize this effect is to minimize the output ripple.

To compensate for valley regulation, it may be desirable to use passive droop. Take the feedback directly from the output side of the inductor and place a small amount of trace resistance between the inductor and output capacitor. This trace resistance should be optimized so that at full load the output droops to near the lower regulation limit. Passive droop minimizes the required output capacitance because the voltage excursions due to load steps are reduced as seen at the load.

The use of 1% feedback resistors contributes up to 1% error. If tighter DC accuracy is required, 0.1% resistors should be used.

The output inductor value may change with current. This will change the output ripple and therefore will have a minor effect on the DC output voltage. The output ESR also affects the output ripple and thus has a minor effect on the DC output voltage.

Applications Information (continued)

Switching Frequency Variations

The switching frequency will vary depending on line and load conditions. The line variations are a result of fixed propagation delays in the on-time one-shot, as well as unavoidable delays in the external MOSFET switching. As V_{IN} increases, these factors make the actual DH on-time slightly longer than the ideal on-time. The net effect is that frequency tends to falls slightly with increasing input voltage.

The switching frequency also varies with load current as a result of the power losses in the MOSFETs and the inductor. For a conventional PWM constant-frequency converter, as load increases the duty cycle also increases slightly to compensate for IR and switching losses in the MOSFETs and inductor. A adaptive on-time converter must also compensate for the same losses by increasing the effective duty cycle (more time is spent drawing energy from V_{IN} as losses increase). The on-time is essentially constant for a given V_{OUT}/V_{IN} combination, to offset the losses the off-time will tend to reduce slightly as load increases. The net effect is that switching frequency increases slightly with increasing load.

PCB Layout Guidelines

As with any switch-mode converter, good PCB layout is essential to achieving high performance. The following guidelines will provide an optimum PCB layout.

The device layout can be considered in four parts;

- Grounding for PGND and AGND
- Power Components
- Low-noise Analog Circuits
- Bypass capacitors

Grounding

- A ground plane layer for PGND is recommended to minimize the effects of switching noise, resistive losses, and to maximize heat removal from the power components.
- A separate ground plane or island should be used for AGND and all associated components. The AGND island should avoid overlapping the switching signals on other layers (DH/DL/BST/LX).
- Connect PGND and AGND together with a zero ohm resistor or copper trace. Make the connection near the AGND and PGND pins of the IC.

Power Components

Use short, wide connections between the power components:

- Input capacitors and high-side MOSFETs
- High-side and Low-side MOSFETs and inductor (LX connection). Use wide copper traces to provide high current carrying capacity and for heat dissipation.
- Inductor and output capacitors
- All PGND connections — the input capacitors, low-side MOSFETs, output capacitors, and the PGND pin of the SC419.
  - An inner layer ground plane is recommended.
  - Each component should have a good, low impedance connection to the ground plane.
  - Place vias to the PGND plane directly near the component pins.
- Use short wide traces for the pin connections from the SC419 (LX, DH, DL and BST). Do not route these traces near the sensitive analog signals (FB, TON, V_{OUT}).

Low-Noise Analog Circuits

Low-noise analog circuits are sensitive circuits that are referenced to AGND. Due to their high impedance and sensitivity to noise, it is important that these circuits be kept away from the switching signals.

- Use a ground plane or solid copper area for AGND. Place all components connected to AGND above this area.
  - Use short direct traces for the AGND connections to all components.
  - Place vias to the AGND plane directly near the component pins.
- Proper routing of the V_{OUT} sense trace is essential since it feeds into the FB resistor divider. Noise on the FB waveform will cause instability and multiple pulsing.

Applications Information (continued)

- Connect the V_{OUT} sense trace directly to the output capacitor or a ceramic bypass capacitor.
- Route this trace over to the VOUT pin, carefully avoiding all switching nets and power components.
- Route this trace in a quiet layer if possible.
- Route this trace away from the switching traces and components, even if the trace is longer. Avoid shorter trace routing through the power switching area.
- If a bypass capacitor is used at the IC side of the trace, it should be placed near the FB resistor divider.

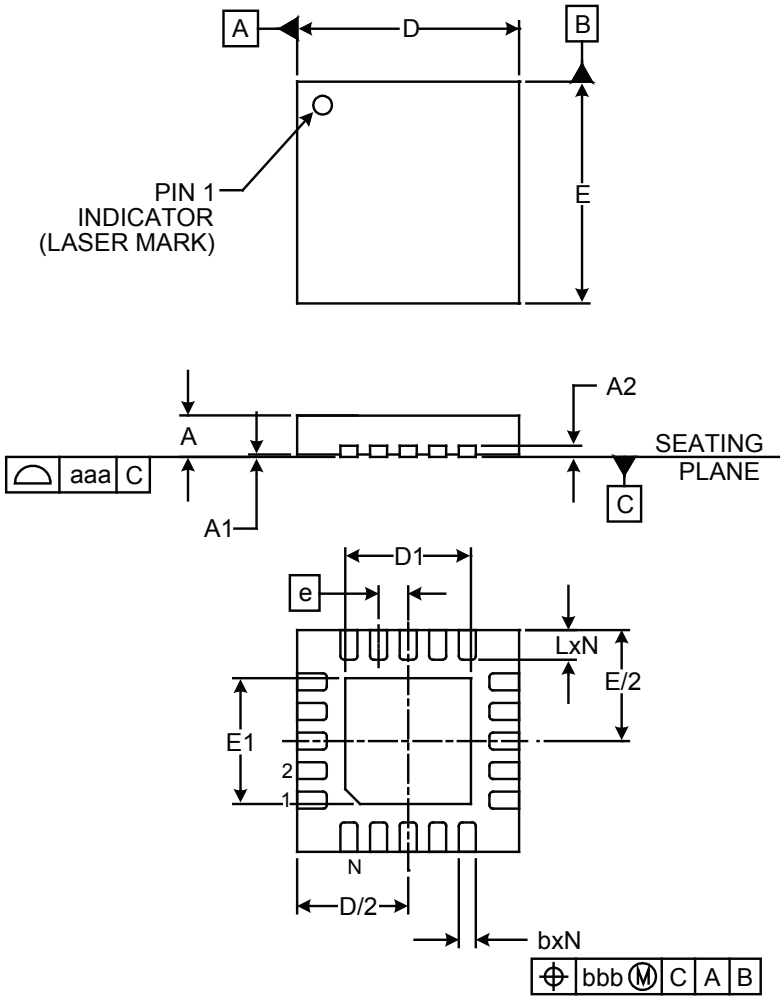
- All components connected to the FB pin must be located near the pin. The FB traces should be kept small and not routed near any noisy switching connections or power components.
- Place the R_{ILIM} resistor near the IC. For an accurate I_{LIM} current sense connection, route the R_{ILIM} trace directly to the drain of the low-side MOSFET (LX). Use an inner routing layer if needed.
- Place the R_{TON} resistor near the TON pin. Route this to the TON trace using a short trace and avoid all switching signals.

Bypass Capacitors

The device requires bypass capacitors for the following pins.

- VDDA pin with respect to AGND. This 100nF minimum capacitor must be placed and routed close to the IC pins, on the same layer as the IC.
- VDDP with respect to PGND. This 1µF minimum capacitor must be placed and routed close to the IC pins and on the same layer as the IC.
- BST pin with respect to LX. This 100nF minimum capacitor must be placed near the IC, on either side of the PCB. Use short traces for the routing between the capacitor and the IC.
- VIN pin with respect to AGND. This 100nF minimum capacitor must be placed and routed close to the IC pins. This capacitor provides noise filtering for the input to the internal on-time circuit.

Outline Drawing — MLPQ-UT20 3x3

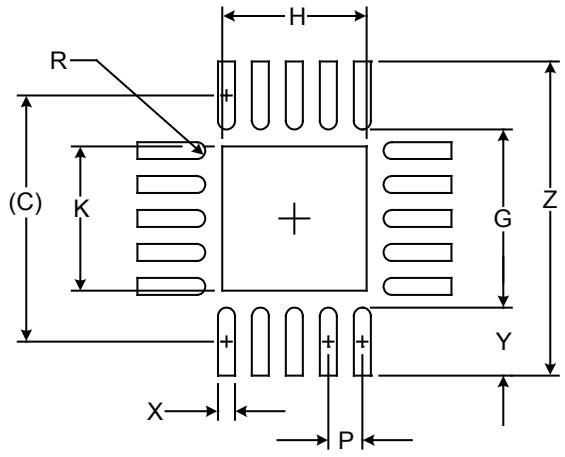


DIMENSIONS						
DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.020	-	.024	0.50	-	0.60
A1	.000	-	.002	0.00	-	0.05
A2		(.006)			(0.1524)	
b	.006	.008	.010	0.15	0.20	0.25
D	.114	.118	.122	2.90	3.00	3.10
D1	.061	.067	.071	1.55	1.70	1.80
E	.114	.118	.122	2.90	3.00	3.10
E1	.061	.067	.071	1.55	1.70	1.80
e		.016 BSC			0.40 BSC	
L	.012	.016	.020	0.30	0.40	0.50
N		20			20	
aaa		.003			0.08	
bbb		.004			0.10	

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
3. DAP is 1.90 x 190mm.

Land Pattern — MLPQ-UT20 3x3



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.114)	(2.90)
G	.083	2.10
H	.067	1.70
K	.067	1.70
P	.016	0.40
R	.004	0.10
X	.008	0.20
Y	.031	0.80
Z	.146	3.70

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
3. THERMAL VIAS IN THE LAND PATTERN OF THE EXPOSED PAD SHALL BE CONNECTED TO A SYSTEM GROUND PLANE. FAILURE TO DO SO MAY COMPROMISE THE THERMAL AND/OR FUNCTIONAL PERFORMANCE OF THE DEVICE.

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