

PM5324 ARROW 1x192

SONET/SDH Transport Framer/Aggregator for OC-48 and OC-192

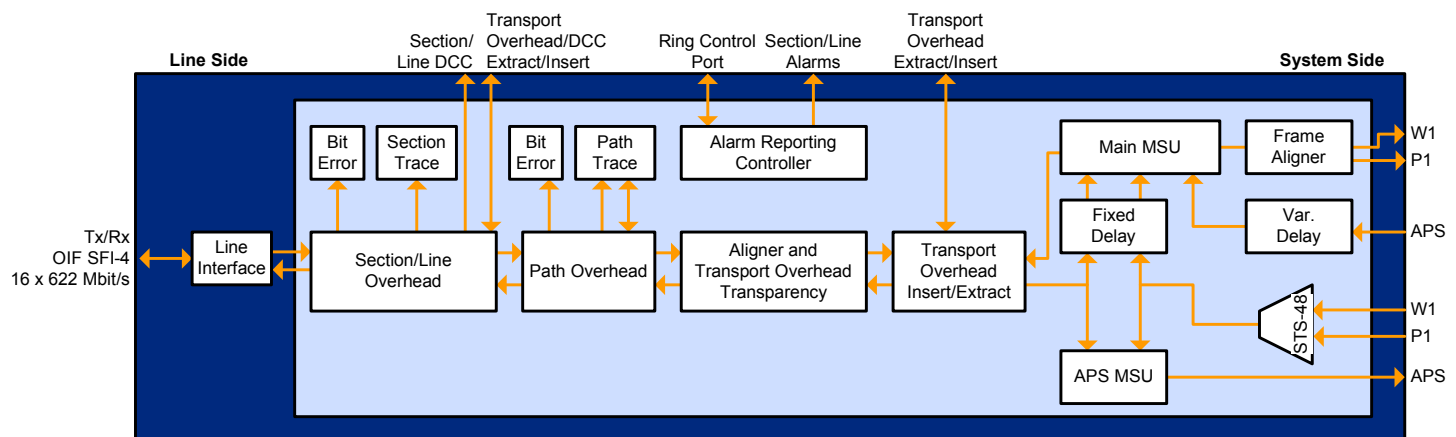
Released Product Brief



Product Overview

- SONET/SDH framer/aggregator for use in channelized STS-192/STM-64 and STS-48/STM-16 applications
- 10 Gbit/s aggregate capacity. The framer can be configured to support:
 - One STS-192/STS-192c / STM-64/STM-64c stream
 - Four STS-48/STS-48c / STM-16/STM-16c streams
- Supports one STS-192/STM-64 stream via a standard OIF SFI-4 interface (duplex 16-bit 622 MHz LVDS) for direct connection to SERDES and CRU/CSU devices
- Supports up to four STS-48/STM-16 via SFI-4 interfaces operating in nibble mode
- Provides working, protect, and APS interfaces for connection across system backplanes. Each interface consists of four ESSI (Extended SONET Serial Interface) RASIO 3G links, operating at 2.488 Gbit/s
- Supports channelized (down to STS-1), concatenated, and arbitrarily concatenated (STS-3cxN) traffic. Changes in traffic configurations are automatically detected
- Terminates (or monitors) SONET/SDH Section, Line, and Path overhead and provides STS-1 granularity frame alignment and pointer processing
- Detects and inserts transport and path BIP-8 errors (B1, B2, B3). Detects signal degrade (SD) and signal fail (SF) threshold crossing alarms for B2 and B3
- Provides overhead passthrough for entire TOH, and re-mapping for B1, B2, M0/M1, and J0 bytes
- Provides dedicated pins to extract and reinsert the entire transport overhead
- Provides dedicated pins to extract section and line DCC
- Supports Automatic Protection Switching:
 - K1/K2 byte filtering and BER monitoring
 - Direct line card APS connections via system side APS ports
- Supports centralized control of SONET/SDH processing by providing in-band status messaging (Transport, Path, and Equipment Status) on the ESSI ports
- Provides independent STS-1 Memory Switching Units (MSU) for combined time-slot interchange (TSI) and muxing functions in transmit and receive directions
- Provides independent STS-1 Memory Switching Units (MSU) at the DROP APS port for grooming traffic to support line card pairing or local traffic termination
- Provides line loopback from the line side receive streams to the transmit streams and supports diagnostic loopback on the system side interface

Block Diagram



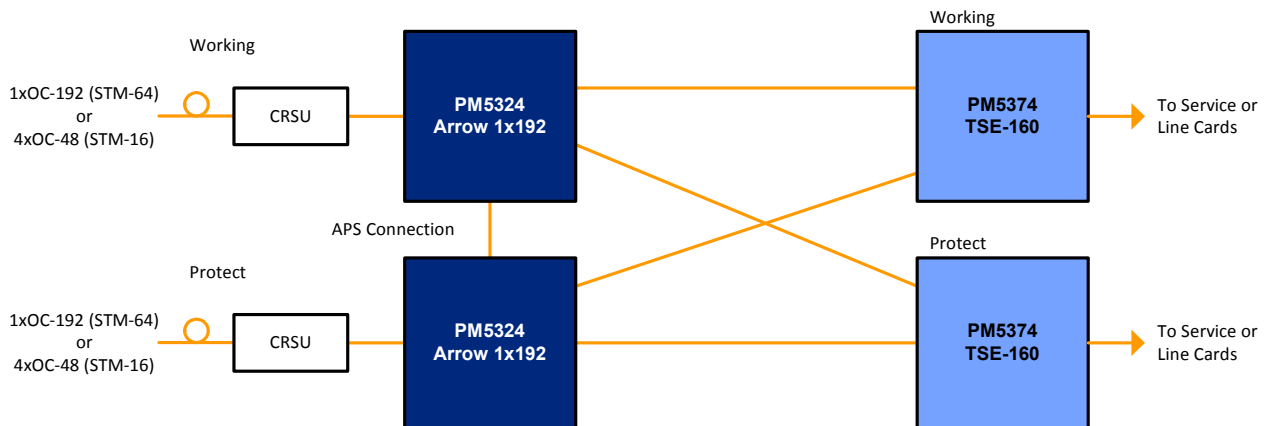
General

- General purpose 16-bit microprocessor interface for configuration, control and status monitoring
- Low power 1.2 V core with 2.5/3.3V I/O
- Standard 5-signal IEEE 1149.1 JTAG test port for boundary scan board test purposes
- 1292-pin FCBGA package

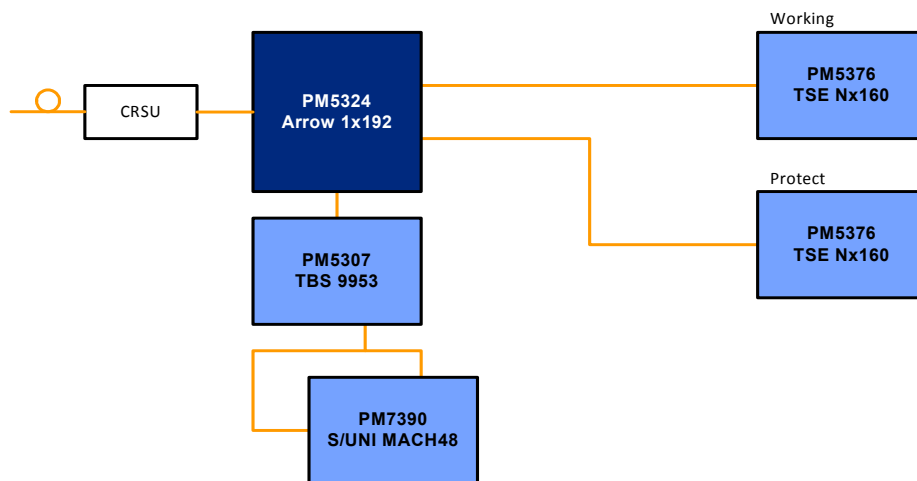
Applications

- Multi Service Provisioning Platforms (MSPP)
- Sub Wavelength Cross Connects
- Add/Drop Multiplexers
- DWDM Platforms
- Channelized Routers and Multi Service Switches

10G Line Card With Local Layer 2 Processing



Cross-Connect



Further Resources

Technology Webpage

www.pmcs.com/products/optical_network/

Technical Documentation

www.pmcs.com/resources/downloads_support.html

About PMC

PMC (Nasdaq:PMCS) is the semiconductor innovator transforming networks that connect, move and store digital content. Building on a track record of technology leadership, we are driving innovation across storage, optical and mobile networks. Our highly integrated solutions increase performance and enable next generation services to accelerate the network transformation. For more information visit www.pmcs.com.

Corporate Head Office:
PMC-Sierra
1380 Bordeaux Drive
Sunnyvale, CA 94089, USA
Tel: 1.408.239.8000
Fax: 1.408.492.1157

Operations Head Office:
PMC-Sierra
8555 Baxter Place
Burnaby, BC V5A 4V7 Canada
Tel: 1.604.415.6000
Fax: 1.604.415.6200

