Nuvoton
Bus Termination Regulator
W83312SN

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1. GENERAL DESCRIPTION

The W83312SN is a linear regulator which provides a power achieves peak 3.0Amp bi-directional sinking and sourcing capability for a high speed bus terminator application. The chip simply implements a stable power supply which tracks half of input power dynamically for bus terminator with a single chip. The W83312SN is promoted with small footprint 8-SOP 150mil power package. With W83312SN design, a high integration, high performance, and cost-effective solution are promoted.

2. FEATURES

2.1. General

- Memory Termination Regulator for DDR1, DDR2, DDR3 and Low Power DDR3
- Sink and Source 3A Peak Current
- Integrated Power MOSFET
- Adjustable V_{OUT} by External Resistors
- Low External Component Count
- Low Output Voltage Offset
- Current Limit Protection
- Over Temperature Protection
- -40°C to 85°C Ambient Operating Temperature Range

2.2. Package

- SOP-8 150mil with Exposed Pad Package
- Lead Free (ROHS Compliant) and Halogen Free

2.3. Applications

- Desktop PCs, Notebooks, and Workstations
- Graphics Card Memory Termination
- Set Top Boxes, Digital TVs and Printers
- Active Termination Buses
- DDR1, DDR2 and DDR3 Memory Systems

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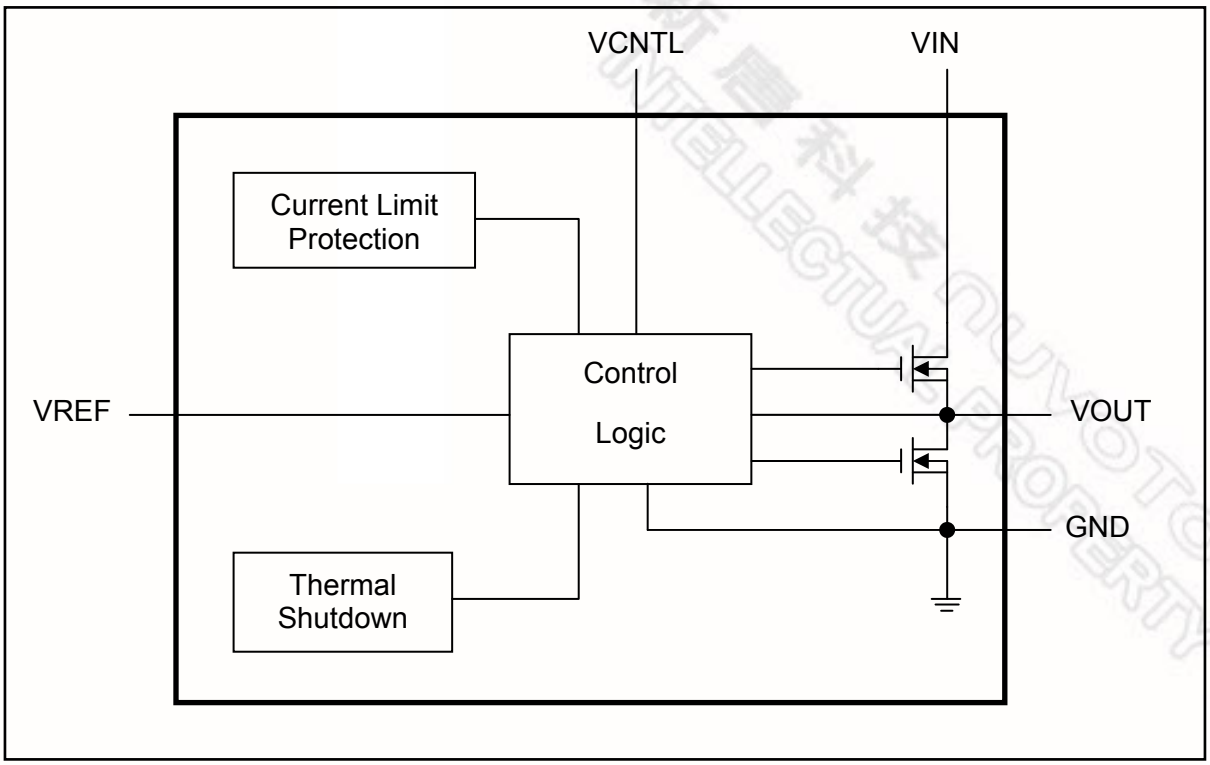
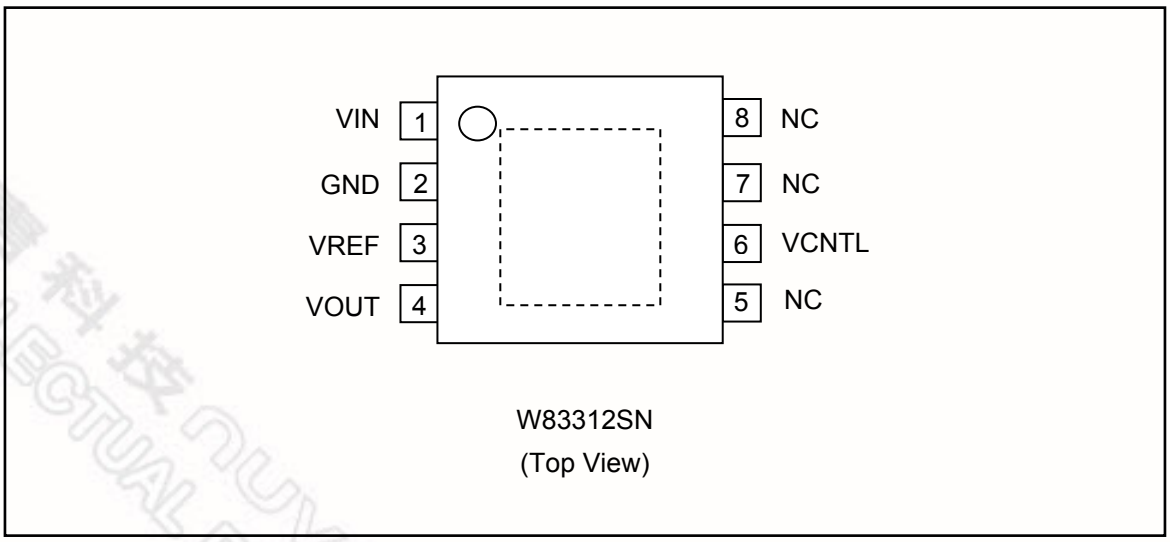
3. BLOCK DIAGRAM



4. PIN CONFIGURATION AND TYPICAL APPLICATION CIRCUIT



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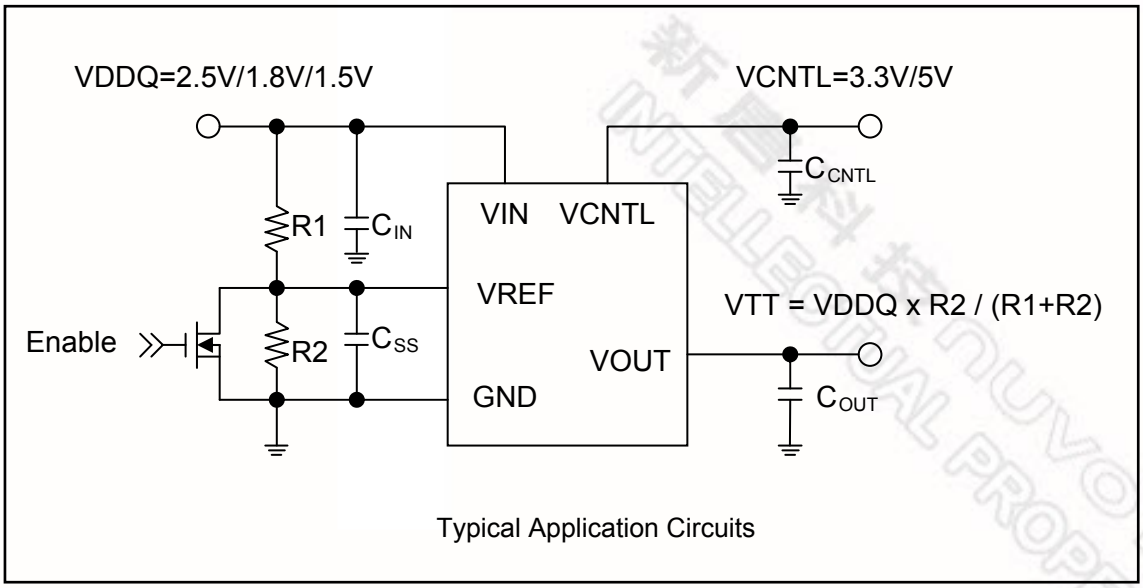


Typical Application Circuits

5. PIN DESCRIPTION

SYMBOL	PIN	I/O	FUNCTION
VIN	1	I	Main power input pin which supplies current to output pin. For lower power dissipation consideration, using VDDQ (Supply voltage for DRAM) as power source is recommended.
VREF	3	I	Internal reference voltage source. Generally, VREF tracks VDDQ/2 for DDR application. Using voltage dividing resistors and capacitor as low pass filter for noise immunity and output voltage soft start is recommended. If using an N-MOSFET as shutdown function, please make sure the sinking current capability can pull down VREF under 0.2V.
VOUT	4	O	Voltage output pin which is regulated to track VREF voltage.
VCNTL	6	I	Power for internal control logic circuitry. A ceramic decoupling capacitor with 1uF is required.
GND	2		Ground. Connect to negative terminal of the output capacitor.
NC	5, 7, 8		No connection.

6. FUNCTIONAL DESCRIPTION

6.1 VTT Sink/Source Regulator

The W83312SN is a sink/source tracking Double Data Rate (DDR) termination regulator specifically designed for low input voltage, low cost and low external component count systems where space is a key application parameter. The W83312SN integrates a high performance, low dropout linear regulator that is capable of both sinking and sourcing current.

6.2 General Regulator

The W83312SN could also serves as a general linear regulator. The W83312SN accepts an external reference voltage at VREF pin and provides output voltage regulated to this reference voltage as shown in Fig.6-1, where

$$VOUT=VEXT \times R2/ (R1+R2)$$

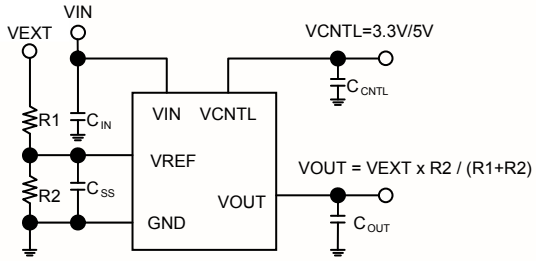


Fig. 6-1

The W83312SN supports wide VREF voltage input range, making it versatile and idea for many types of low power LDO applications. The dropout voltage is the input voltage minus output voltage that produces 2% decrease in output voltage, where

$$VIN_{MIN}=V_{DROPOUT} + VOUT$$

The output voltage range depends on VCNTL voltage and output loading which means higher VCNTL voltage can support higher output voltage and higher output loading.

Fig.6-2 and Table 6-1 show that the relationships among VOUT, $V_{DROPOUT}$ and IOUT when VCNTL=5V. For example, if VOUT=3.4V, the maximum output loading is 1.5A with 0.25V dropout voltage and the minimum VIN is 3.65V. The *Max* column in the table means the minimum dropout voltage needed in worst conditions. Choose suitable VIN voltage to obtain better efficiency.

VCNTL=5V				
Parameter	**Conditions**	**Typ.**	**Max**	**Unit**
Dropout Voltage	IOUT=1A, 0.6V≦ VOUT ≦3.4V	0.15	0.3	V
	IOUT=1.5A, 0.6V≦ VOUT ≦3.4V	0.25	0.5	
	IOUT=2A, 0.6V≦ VOUT ≦3.2V	0.35	0.7	
	IOUT=2.5A, 0,8V≦ VOUT ≦3V	0.5	1	

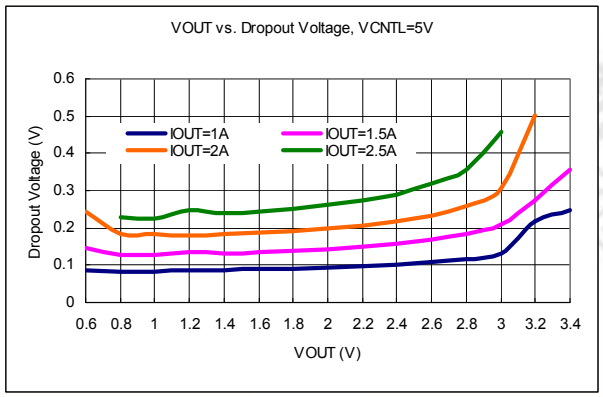


Fig. 6-2

Fig.6-3 and Table 6-2 show that the relationships among VOUT, $V_{DROPOUT}$ and IOUT when VCNTL=3.3V.

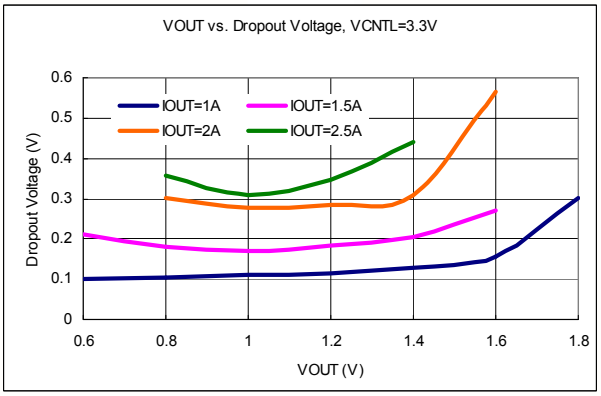


Fig. 6-3

VCNTL=3.3V				
Parameter	**Conditions**	**Typ.**	**Max**	**Unit**
Dropout Voltage	IOUT=1A, 0.6V≦ VOUT ≦1.8V	0.35	0.7	V
	IOUT=1.5A, 0.6V≦ VOUT ≦1.6V	0.35	0.7	
	IOUT=2A, 0.6V≦ VOUT≦ 1.6V	0.6	1.2	
	IOUT=2.5A, 0.8V≦ VOUT≦ 1.4V	0.45	0.9	

Table 6-1

Table 6-2

6.3 Shutdown Function

When the external reference voltage at VREF pin is under shutdown threshold, the internal regulator will be turned off and VOUT is at High-Z state.

6.4 Over Current Protection

The W83312SN provides a current limit circuitry, which monitors the output current and controls NMOS's gate voltage to limit the output current at 3.5A, typically.

6.5 Over Temperature Protection

The W83312SN monitors its junction temperature. If the device junction temperature exceeds its threshold value, typically 165°C, the VOUT is shut off. The shutdown is a non-latch protection.

6.6 Thermal Design

Since the W83312SN is a linear regulator, the VOUT current flows in both source and sink directions, thereby dissipating power from the device. When the device is sourcing current, the

voltage difference between VIN and VOUT times I_{OUT} current becomes the power dissipation as shown in below equation.

$$P_{DISS_SOURCE} = (VIN\text{-}VOUT) \times I_{OUT_SOURCE}$$

In this case, if VIN is connected to an alternative power supply lower than the VDDQ voltage, overall power loss can be reduced. For the sink phase, VOUT voltage is applied across the internal LDO regulator and the power dissipation, P_{DISS_SINK} can be calculated by below equation.

$$P_{DISS_SINK} = VOUT \times I_{OUT_SINK}$$

Because the device does not sink and source current at the same time and the I_{OUT} current may vary rapidly with time, the actual power dissipation should be the time average of the above dissipations over the thermal relaxation duration of the system. Another source of power consumption is the current used for the internal current control circuitry form VCNTL supply and the VIN supply. This can be estimate as 10mW or less during normal operating conditions. The power must be effectively dissipated from the package.

Maximum power dissipation allowed by the package is calculated by below equation.

$$P_{PKG} = [\, T_{J(MAX)} - T_{A(MAX)}] / \theta_{JA}$$

, where

- $T_{J(MAX)}$ is +125°C
- $T_{A(MAX)}$ is the maximum ambient temperature in the system
- θ_{JA} is the thermal resistance form junction to ambient

6.7 Input Capacitor

Depending on the trace impedance between the VIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the VIN input capacitor. Use a 100uF (or greater) capacitor to supply this transient charge. Provide more input capacitance as more output capacitance is used at VOUT.

6.8 Output Capacitor

For stable operation, the total capacitance of the VOUT terminal must be greater than 100uF. Attach two or more capacitors in parallel to minimize the effect of equivalent series resistance (ESR) and equivalent series inductance (ESL).

6.9 Layout Consideration

Consider the following points before starting the W83312SN layout design. Fig. 6-4 shows the suggestion of minimum land pattern. Fig. 6-5 shows the recommended PCB layout. Using “dog bone” copper patterns on the top layer can increase efficiency of heat dissipating.

- The input bypass capacitor for VIN should be placed as close as possible to the pin with short and wide connections.
- The output capacitor for VOUT should be placed close to the pin with short and wide connection in order to avoid ESR and/or ESL trace inductance.
- In order to effectively remove heat from the package, properly prepare the thermal land. Apply solder directly to the package’s thermal pad. The wide traces of component and the side copper connected to the thermal land pad help to dissipate heat. The thermal land connected to the ground plane could also be used to help dissipation.

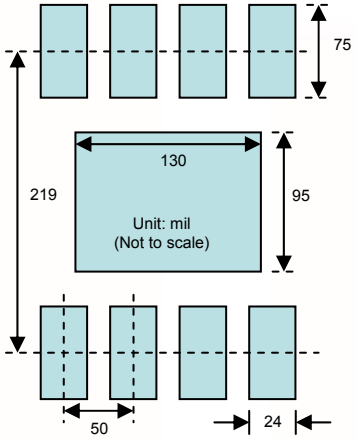


Fig. 6-4

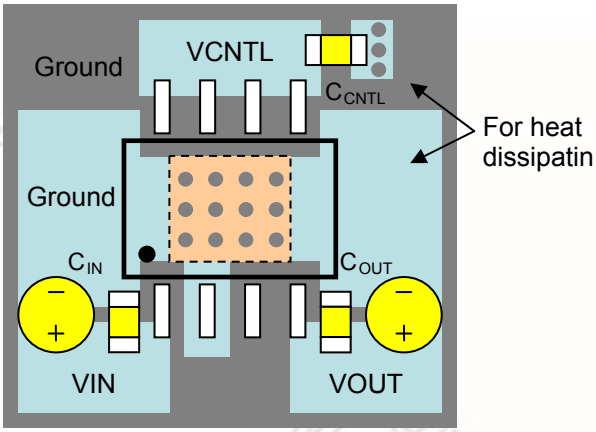


Fig. 6-5

7. ELECTRICAL CHARACTERISTIC

7.1 Absolute Maximum Ratings (Note1)

ITEM	SYMBOL	RATING	UNIT
Input Voltage	VIN	-0.3 to 7	V
Control Logic Input Voltage	VCNTL	-0.3 to 7	V
Reference Voltage	VREF	-0.3 to 5	V
Electrostatic discharge protection (Note2)	Human Body Mode	±2	kV
	Machine Mode	±200	V
	Latch-Up	±100	mA
Storage Temperature Range		-65 to 150	°C

7.2 Thermal Information

ITEM	RATING	UNIT
Power Dissipation, P_D @ T_A=25°C	Internal Limited	W
Package Thermal Resistance, ESOP8, θ_{JA}	75	°C/W

7.3 Recommended Operating Conditions

ITEM	SYMBOL	MIN	MAX	UNIT
Input Voltage	VIN	1.2	5.5	V
	VCNTL	3	5.5	
	VREF	0.6	3.3	V
Continuous Output Current	Sourcing	0	2.5	A
	Sinking	0	2.5	
Peak Output Current	Sourcing	0	3.0	A
	Sinking	0	3.0	

Operating Temperature Range		-40	85	°C
Junction Temperature Range (Note3)		-40	125	°C

7.4 Electrical Characteristics

Typicals and limits appearing in normal type apply for Tj = 25°C. Limits appearing in **Boldface** type apply over the entire junction temperature range for operation, -40°C to 85°C (Note4). VCNTL= 3.3V/5V, VIN=2.5V/1.8V/1.5V, VREF=1.25V/0.9V/0.75V, C_{OUT}=100uF, all voltage outputs unloaded (unless otherwise noted).

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Input						
VCNTL Operating Current	I_{CNTL}	I_{OUT}=0A, VCNTL=3.3V		0.5	**0.7**	mA
		I_{OUT}=0A, VCNTL=5V		0.7	**1**	
VIN Operating Current	I_{VIN}	I_{OUT}=0A, VCNTL=3.3V		0.3	**0.5**	mA
		I_{OUT}=0A, VCNTL=5V		0.3	**0.5**	
VCNTL Quiescent Current in Shutdown Mode	I_{SD_CNTL}	VREF < 0.2V, VCNTL=3.3V		60	**90**	uA
		VREF < 0.2V, VCNTL=5V		60	**90**	
VIN Quiescent Current in Shutdown Mode	I_{SD_VIN}	VREF < 0.2V	**-1**	0	**1**	uA
VREF Leakage Current	I_{IH}	VREF=3.3V	**-1**	0	**1**	uA
	I_{IL}	VREF=0V	**-1**	0	**1**	
Output (DDR1 / DDR2 / DDR3)						
Output Offset Voltage (VREF-VOUT)	V_{OS}	I_{OUT}=0A	**-5**		**5**	mV
Load Regulation (VREF-VOUT)	ΔV_L	I_{OUT}=0 → +2.5A (Note5)	**-20**		**20**	mV
		I_{OUT}=0 → -2.5A (Note5)	**-20**		**20**	
Protection						
Current Limit	I_{LIM}	In any VIN	**±3**	±3.5	**±4.5**	A
Thermal Shutdown Temperature	T_{SD}	3.3V < VCNTL < 5V (Note6)	150	165	175	°C
Thermal Shutdown Hysteresis	ΔT_{SD}	3.3V < VCNTL < 5V		30		°C
VREF Shutdown Mode						
Shutdown Threshold	V_{IH}	Enable	**0.6**			V
	V_{IL}	Disable			**0.2**	

Note1. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Note2. Devices are ESD sensitive. Handling precaution recommended.

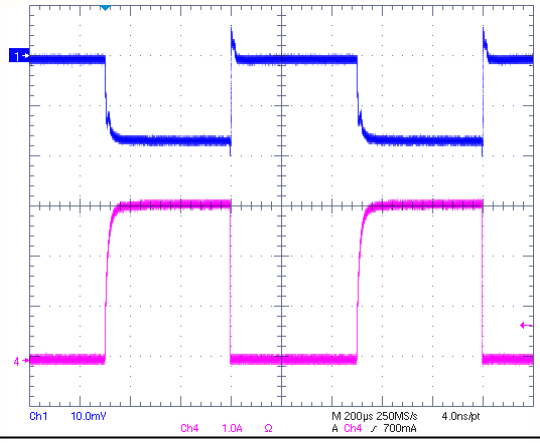
Note3. At elevated temperatures, devices must be de-rated based on thermal resistance. The device in the ESOP-8 package must be de-rated at θ_{JA}=75°C/W junction to ambient with minimum PCB footprint.

Note4. Limits are 100% production tested at 25˚C. Limits over operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate average outgoing quality level.

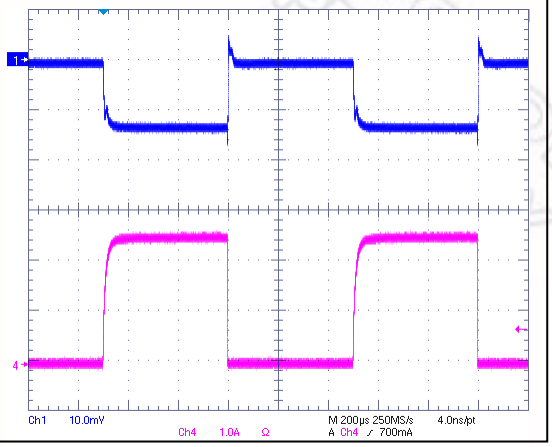
Note5. VOUT load regulation is tested by using a 10ms period and 50% duty cycle current pulse.

Note6. The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction to ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. exceeding the maximum allowable power dissipation will cause excessive die temperature and the regulator will go into thermal shutdown. Ensured by design, no production tested.

8. TYPICAL OPERATING WAVEFORMS



VIN=2.5V, VCNTL=3.3V, VOUT=1.25V @ 3A Sourcing



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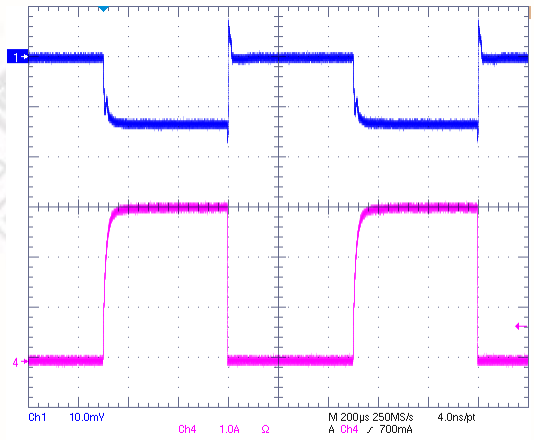

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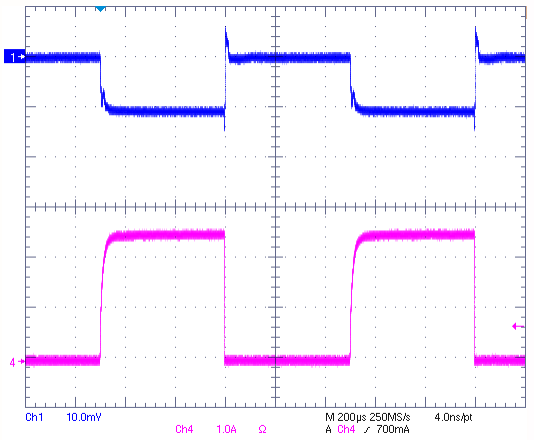

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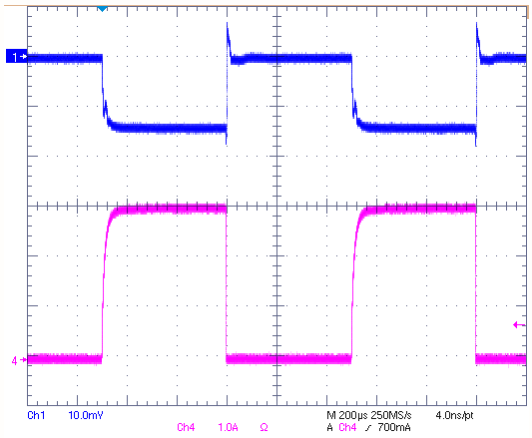
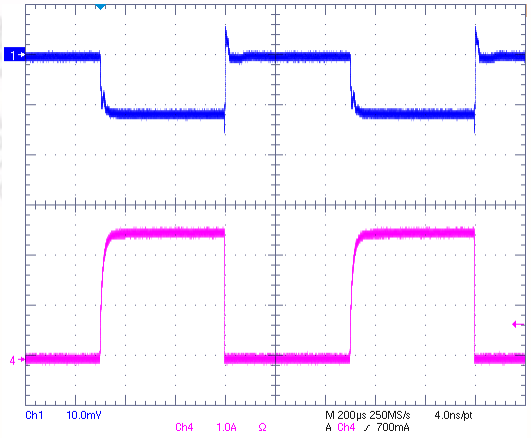
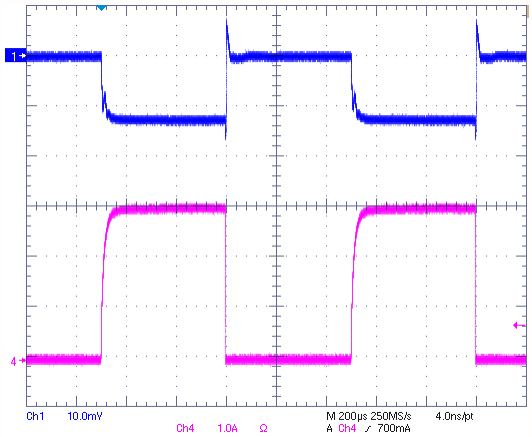


VIN=1.8V, VCNTL=3.3V, VOUT=0.9V @ 3A Sourcing



VIN=1.8V, VCNTL=3.3V, VOUT=0.9V @ 2.5A Sourcing



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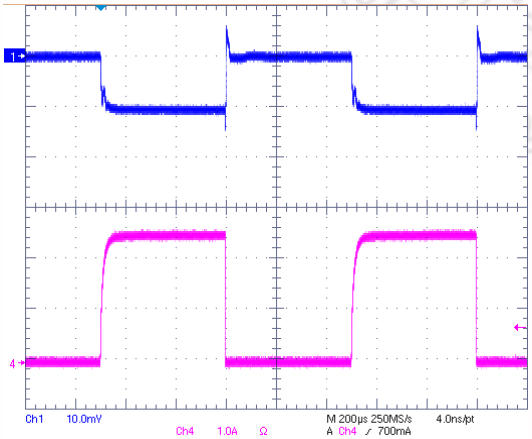

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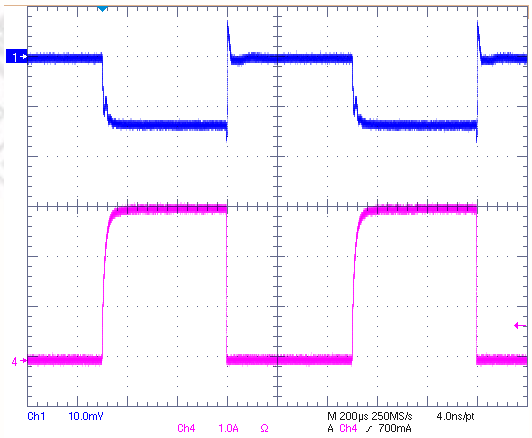
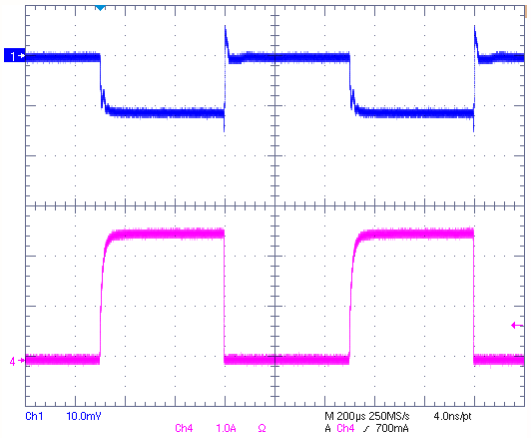
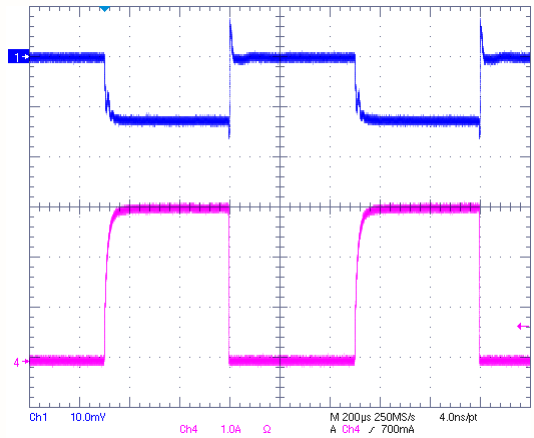


VIN=1.5V, VCNTL=3.3V, VOUT=0.75V @ 3A Sourcing



VIN=1.5V, VCNTL=3.3V, VOUT=0.75V @ 2.5A Sourcing



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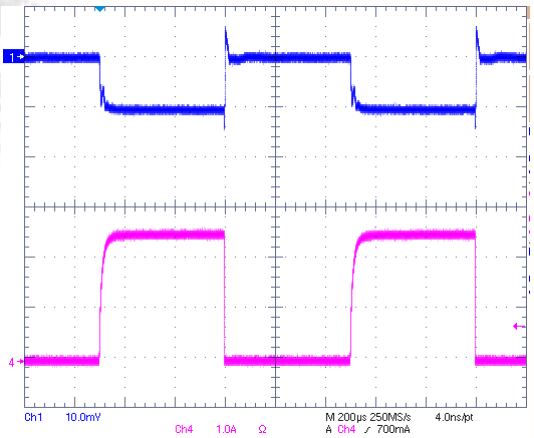

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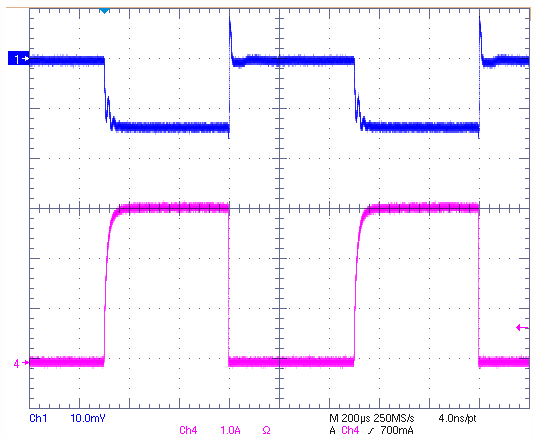

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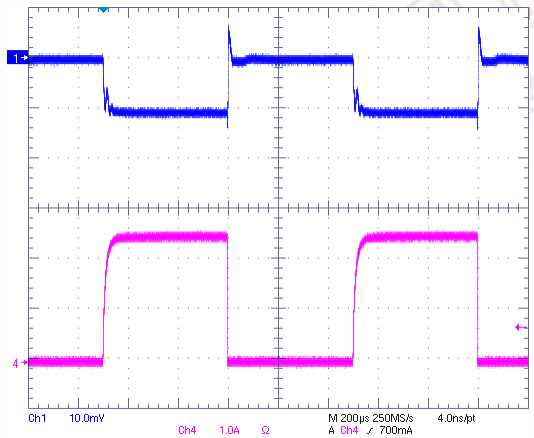

VIN=1.2V, VCNTL=3.3V, VOUT=0.6V @ 2.5A Sourcing

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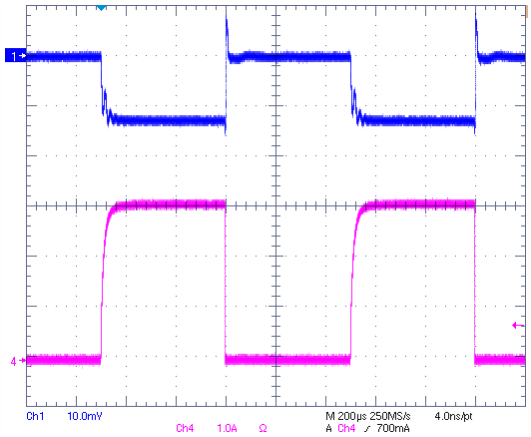

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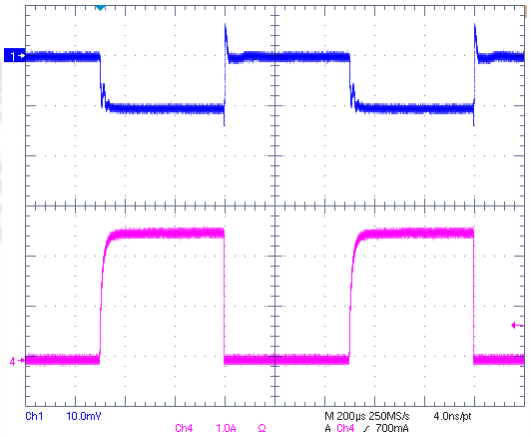
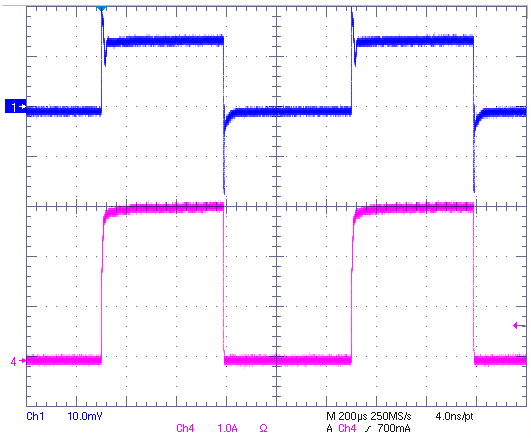
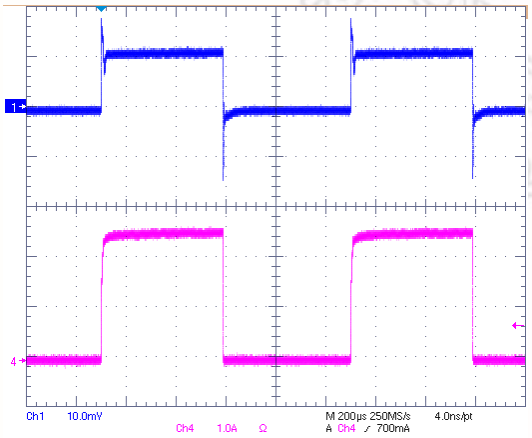


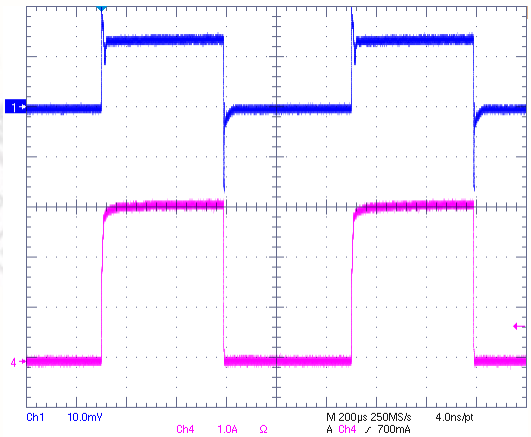
VIN=1.2V, VCNTL=5V, VOUT=0.6V @ 2.5A Sourcing



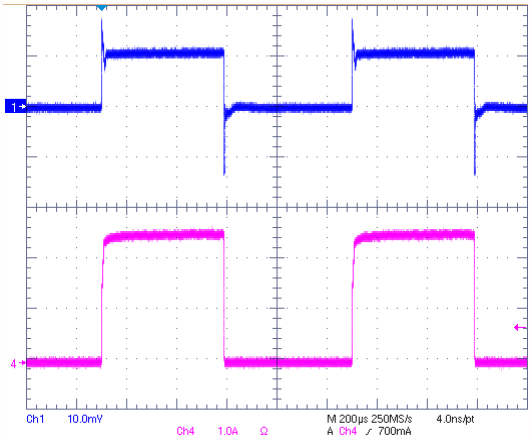
VIN=2.5V, VCNTL=3.3V, VOUT=1.25V @ 3A Sinking



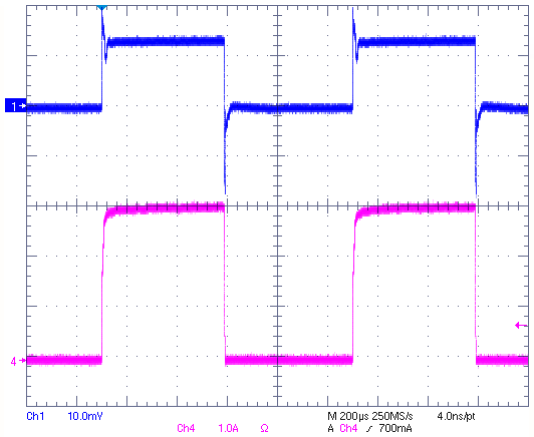
VIN=2.5V, VCNTL=3.3V, VOUT=1.25V @ 2.5A Sinking



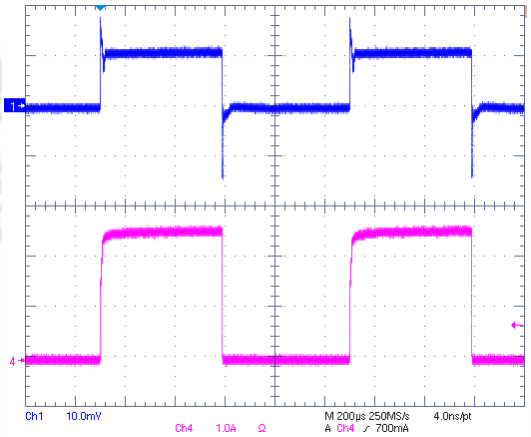
VIN=2.5V, VCNTL=5V, VOUT=1.25V @ 3A Sinking



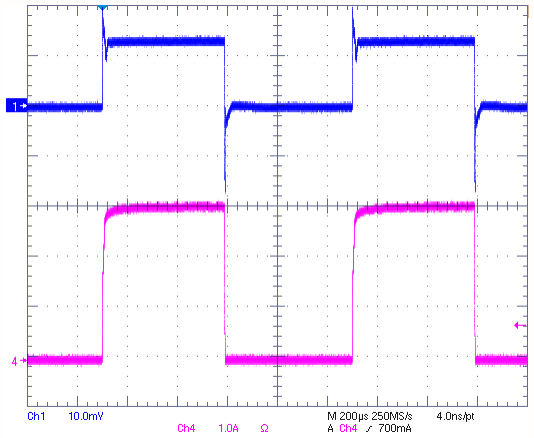
VIN=2.5V, VCNTL=5V, VOUT=1.25V @ 2.5A Sinking



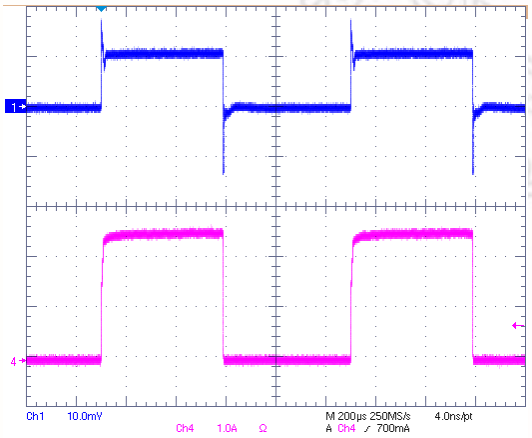
VIN=1.8V, VCNT3O.9V @ 3A Sinking



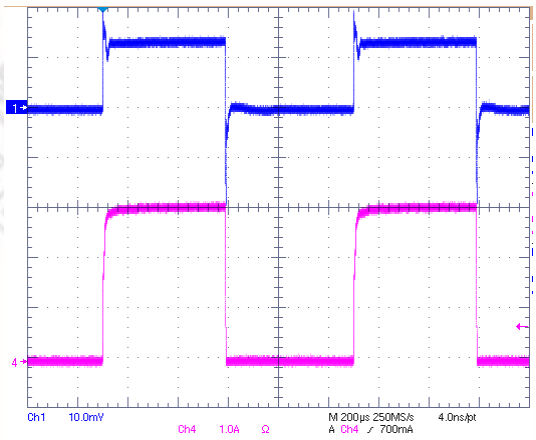
VIN=1.8V, VCNTL=3.3V, VOUT=0.9V @ 2.5A Sinking



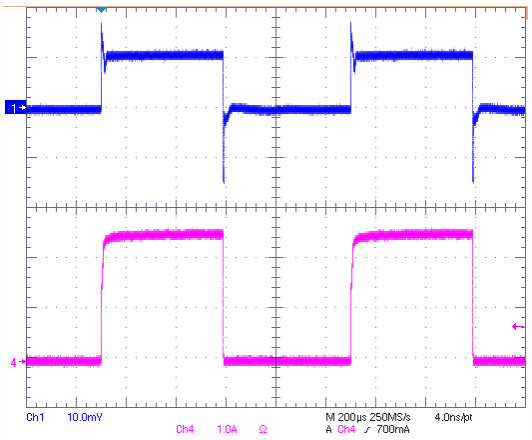
VIN=1.8V, VCNTL=5V, VOUT=0.9V @ 3A Sinking



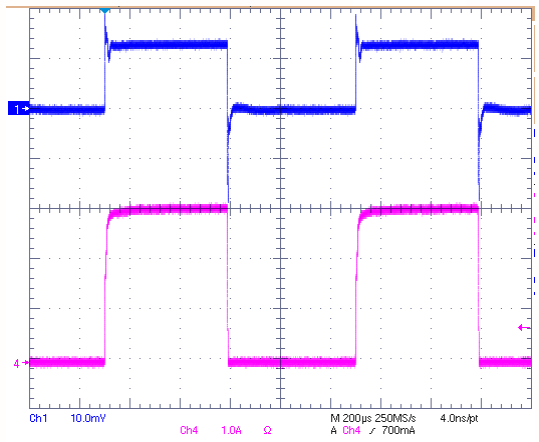
VIN=1.8V, VCNTL=5V, VOUT=0.9V @ 2.5A Sinking



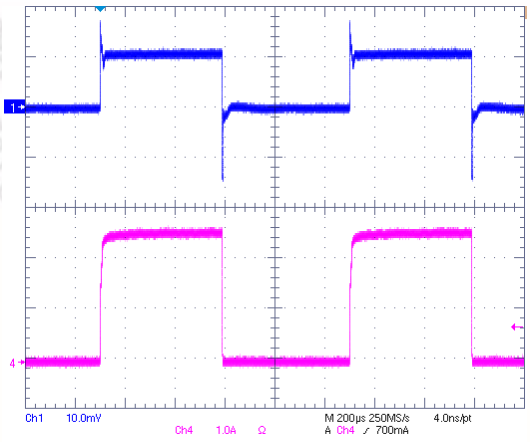
VIN=1.5V, VCNTL=3.3V, VOUT=0.75V @ 3A Sinking



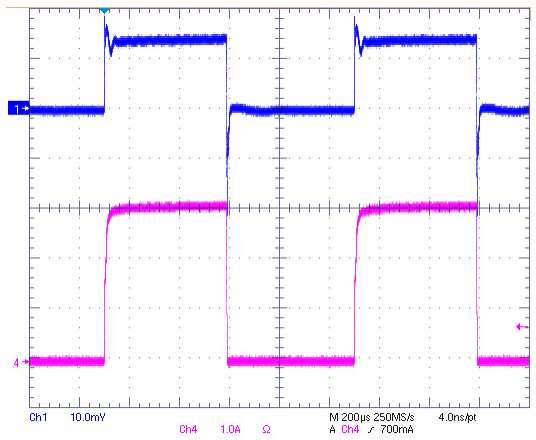
VIN=1.5V, VCNTL=3.3V, VOUT=0.75V @ 2.5A Sinking



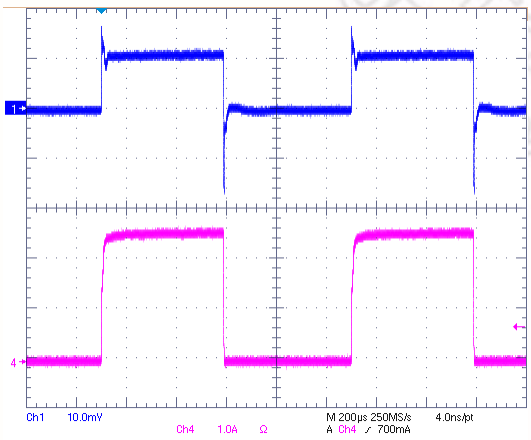
VIN=1.5V, VCNTL=5V, VOUT=0.75V @ 3A Sinking



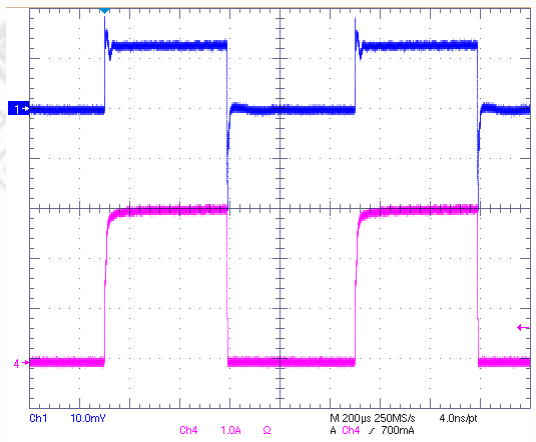
VIN=1.5V, VCNTL=5V, VOUT=0.75V @ 2.5A Sinking



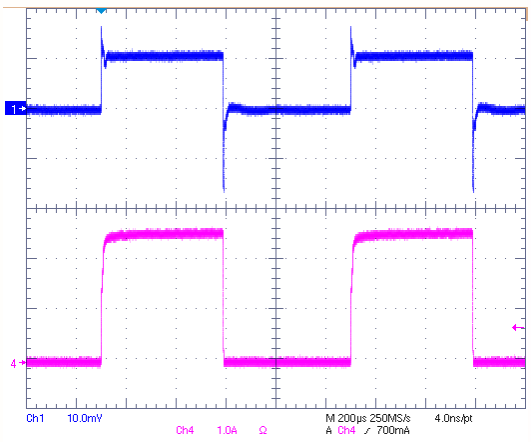
VIN=1.2V, VCNTL=3.3V, VOUT=0.6V @ 3A Sinking



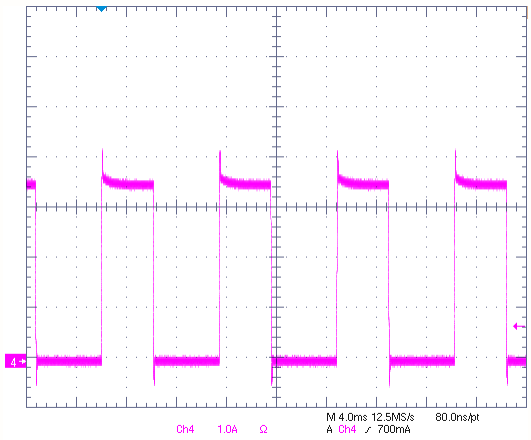
VIN=1.2V, VCNTL=3.3V, VOUT=0.6V @ 2.5A Sinking



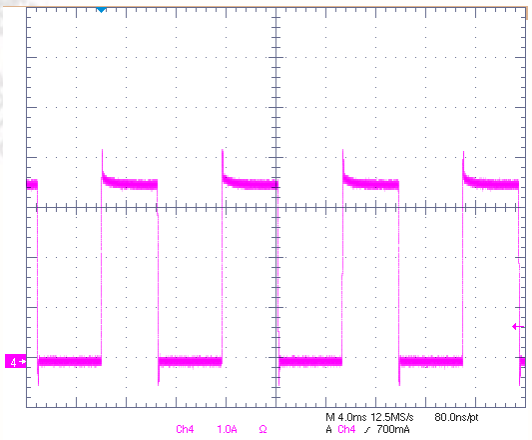
VIN=1.2V, VCNTL=5V, VOUT=0.6V @ 3A Sinking



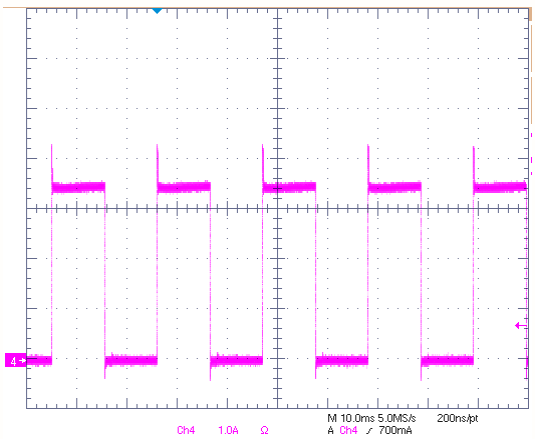
VIN=1.2V, VCNTL=5V, VOUT=0.6V @ 2.5A Sinking



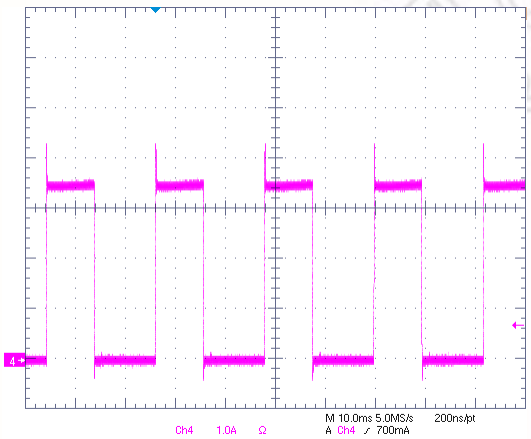
VIN=2.5V, VCNTL=3.3V, VOUT=1.25V, VOUT short to GND



VIN=2.5V, VCNTL=5V, VOUT=1.25V, VOUT short to GND



VIN=2.5V, VCNTL=3.3V, VOUT=1.25V, VOUT short to VIN



VIN=2.5V, VCNTL=5V, VOUT=1.25V, VOUT short to VIN

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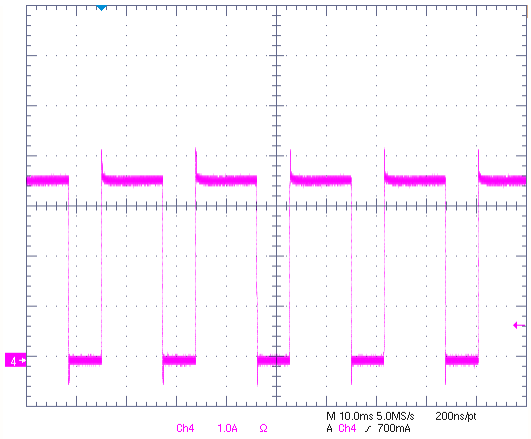
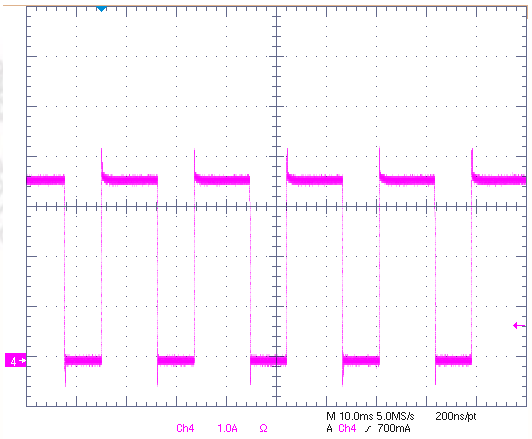
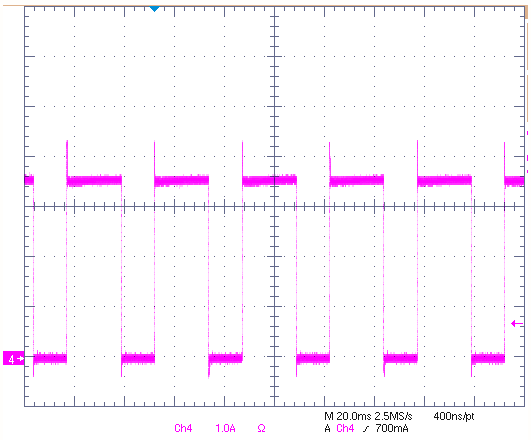


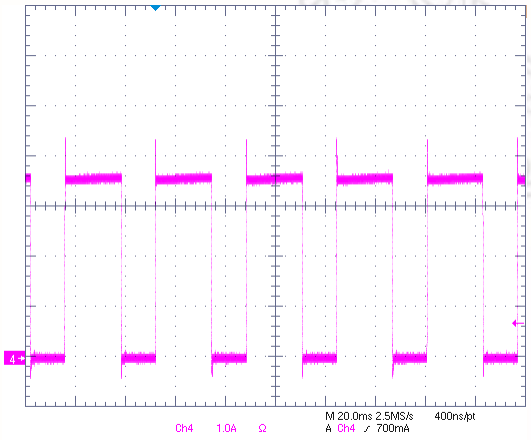
VIN=1.8V, VCNTL=3.3V, VOUT=0.9V, VOUT short to GND



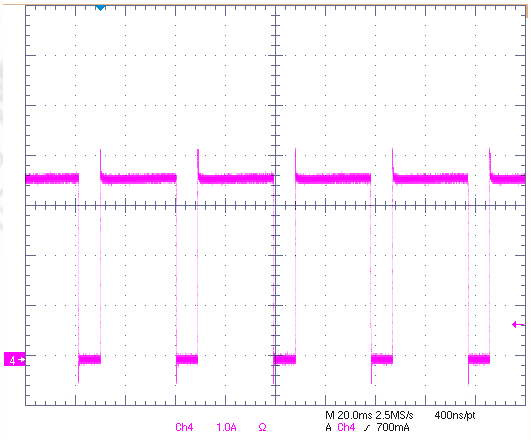
VIN=1.8V, VCNTL=5V, VOUT=0.9V, VOUT short to GND



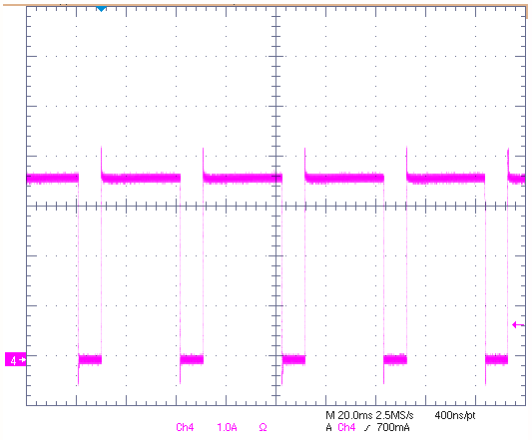
VIN=1.8V, VCNTL=3.3V, VOUT=0.9V, VOUT short to VIN



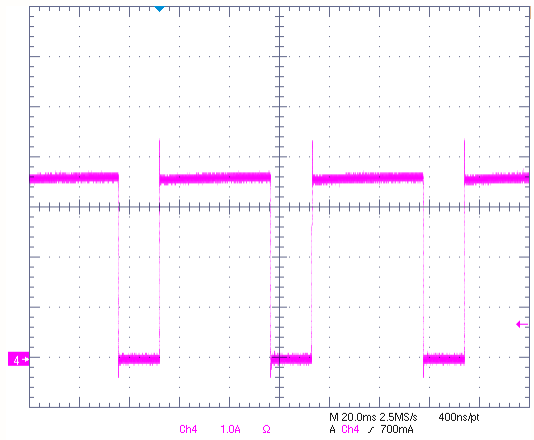
VIN=1.8V, VCNTL=5V, VOUT=0.9V, VOUT short to VIN



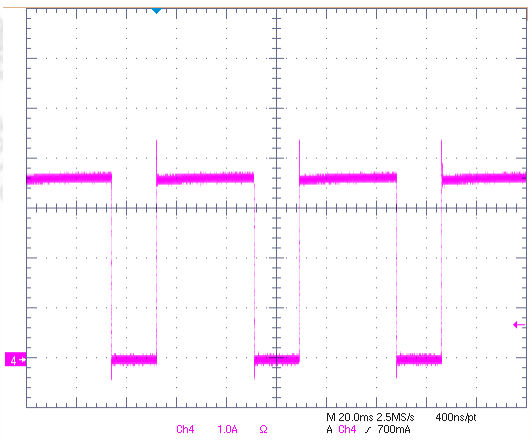
VIN=1.5V, VCNTL=3.3V, VOUT=0.75V, VOUT short to GND



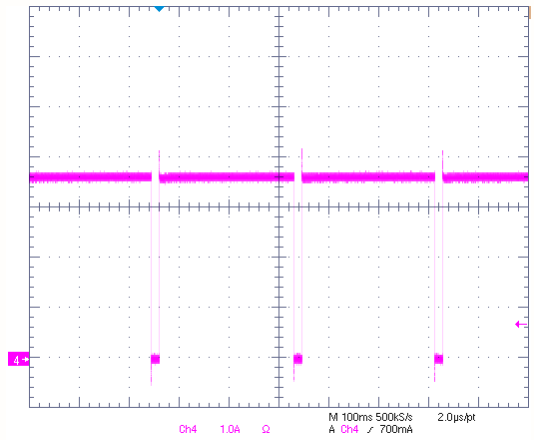
VIN=1.5V, VCNTL=5V, VOUT=0.75V, VOUT short to GND



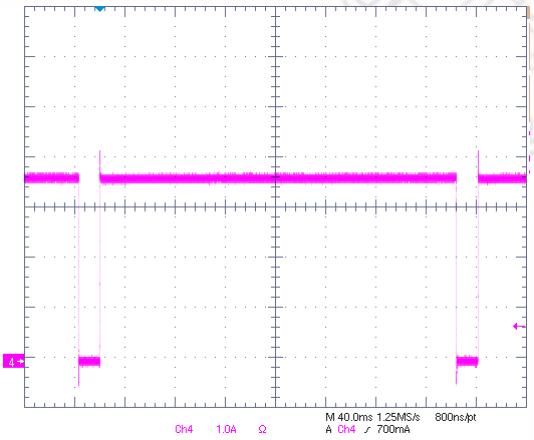
VIN=1.5V, VCNTL=3.3V, VOUT=0.75V, VOUT short to VIN



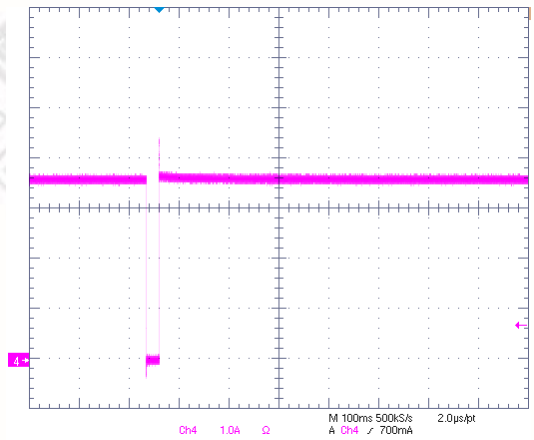
VIN=1.5V, VCNTL=5V, VOUT=0.75V, VOUT short to VIN



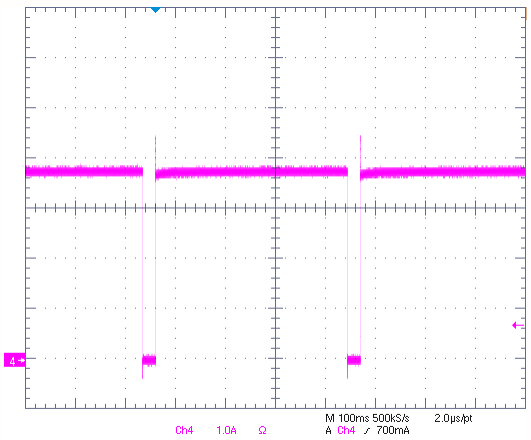
VIN=1.2V, VCNTL=3.3V, VOUT=0.6V, VOUT short to GND



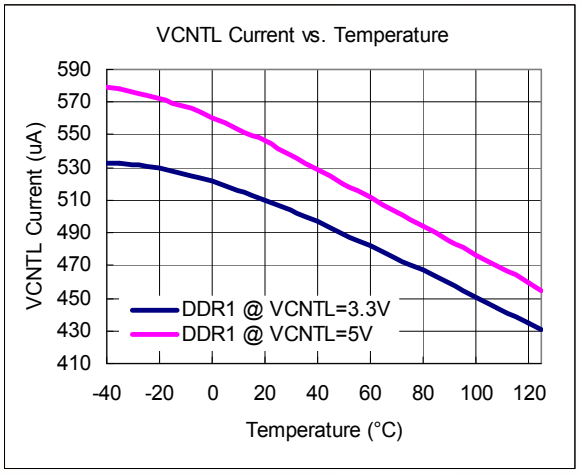
VIN=1.2V, VCNTL=5V, VOUT=0.6V, VOUT short to GND

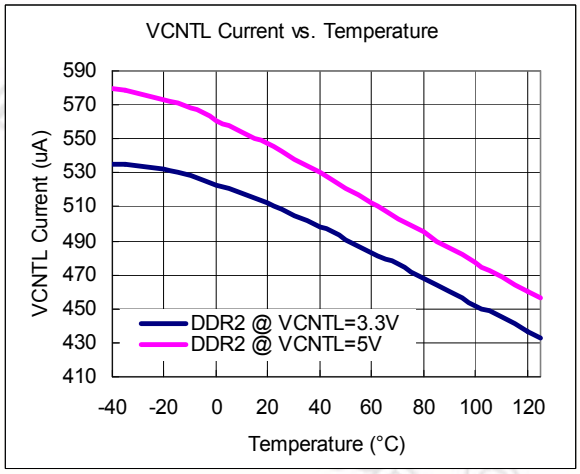


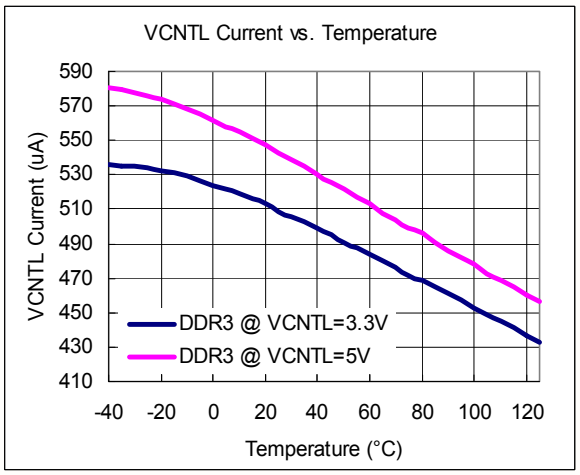
VIN=1.2V, VCNTL=3.3V, VOUT=0.6V, VOUT short to VIN

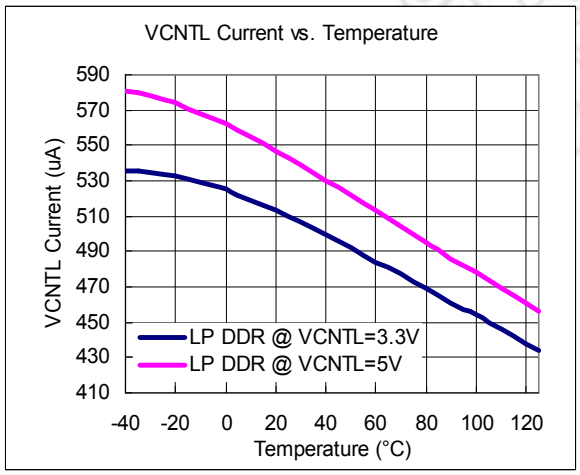


VIN=1.2V, VCNTL=5V, VOUT=0.6V, VOUT short to VIN









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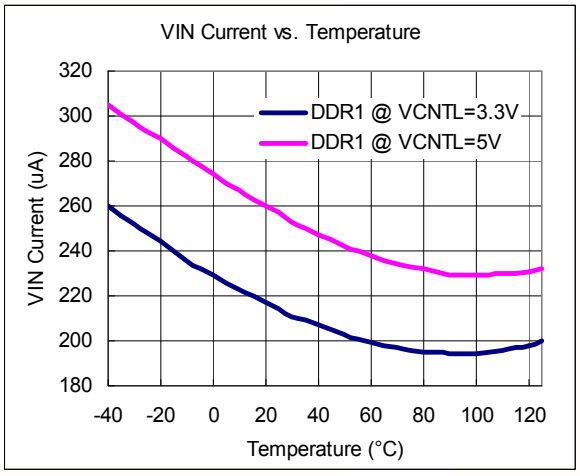
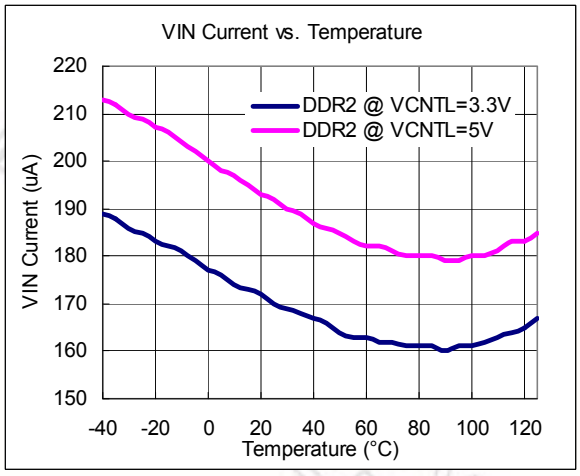
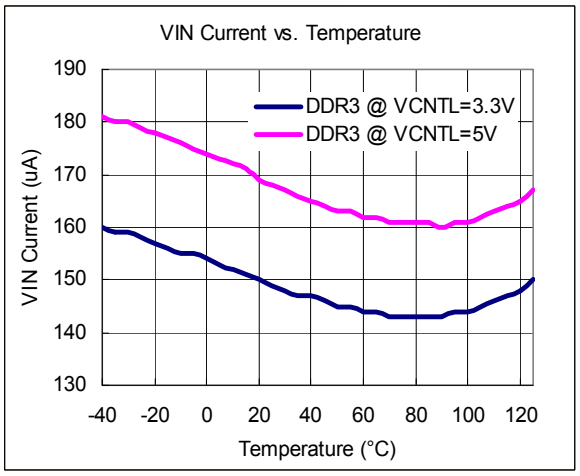
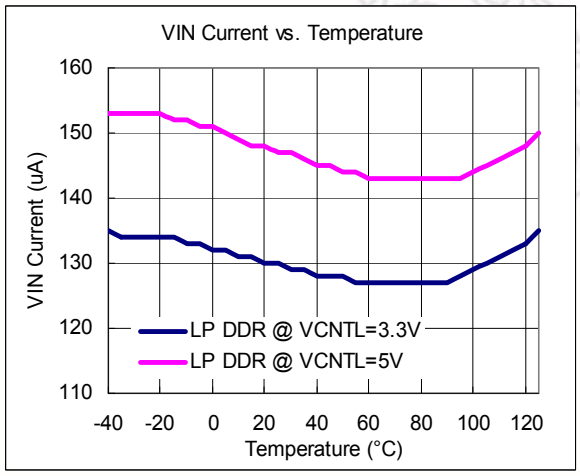
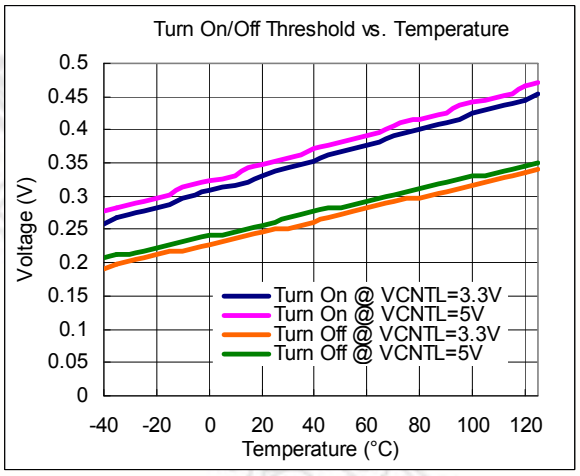
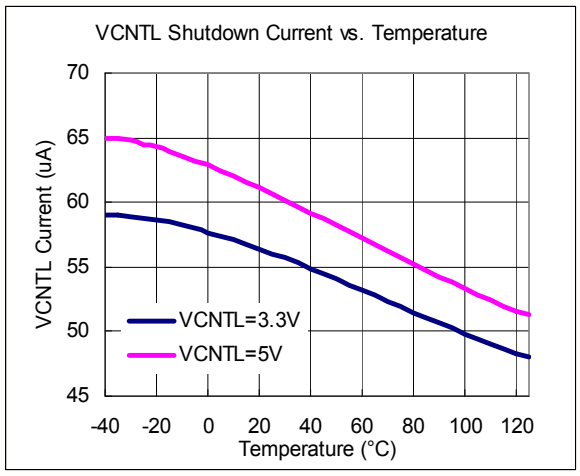

VIN Current vs. Temperature
VIN Current (uA)
320
300
280
260
240
220
200
180
-40 -20 0 20 40 60 80 100 120
Temperature (°C)
DDR1 @ VCNTL=3.3V
DDR1 @ VCNTL=5V

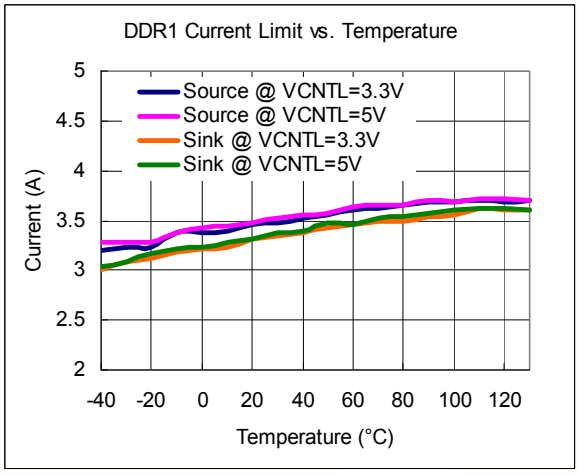

VIN Current vs. Temperature
VIN Current (uA)
220
210
200
190
180
170
160
150
-40 -20 0 20 40 60 80 100 120
Temperature (°C)
DDR2 @ VCNTL=3.3V
DDR2 @ VCNTL=5V

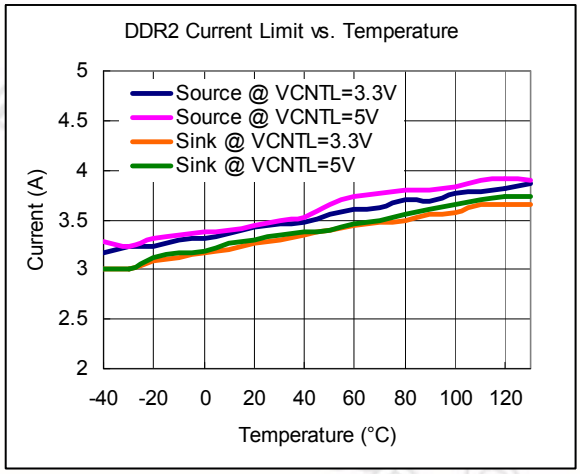

VIN Current vs. Temperature
VIN Current (uA)
190
180
170
160
150
140
130
-40 -20 0 20 40 60 80 100 120
Temperature (°C)
DDR3 @ VCNTL=3.3V
DDR3 @ VCNTL=5V

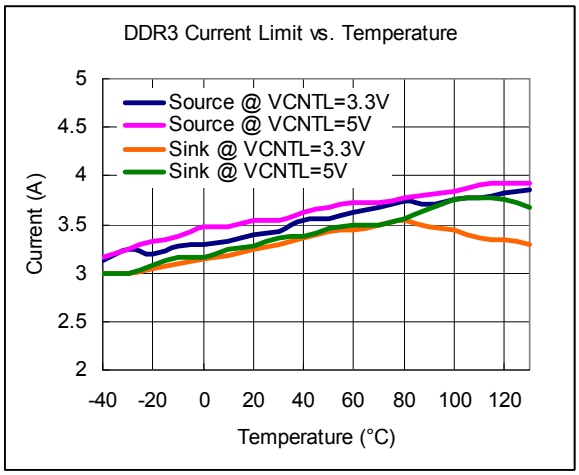

VIN Current vs. Temperature
VIN Current (uA)
160
150
140
130
120
110
-40 -20 0 20 40 60 80 100 120
Temperature (°C)
LP DDR @ VCNTL=3.3V
LP DDR @ VCNTL=5V

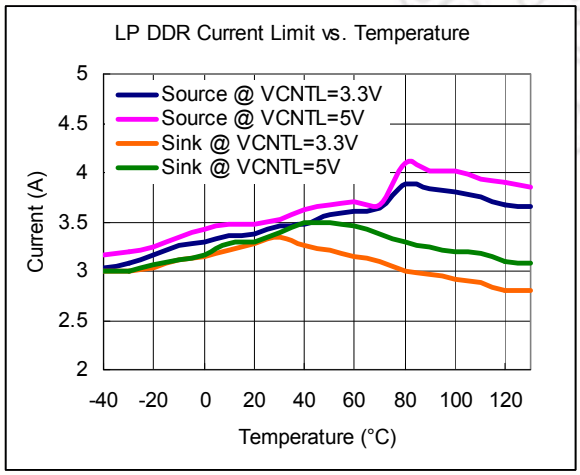

Turn On/Off Threshold vs. Temperature
Voltage (V)
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
-40 -20 0 20 40 60 80 100 120
Temperature (°C)
Turn On @ VCNTL=3.3V
Turn On @ VCNTL=5V
Turn Off @ VCNTL=3.3V
Turn Off @ VCNTL=5V


VCNTL Shutdown Current vs. Temperature
VCNTL Current (uA)
70
65
60
55
50
45
-40 -20 0 20 40 60 80 100 120
Temperature (°C)
VCNTL=3.3V
VCNTL=5V









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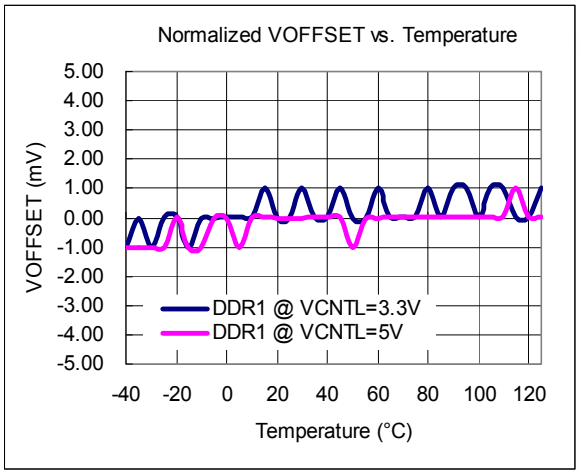

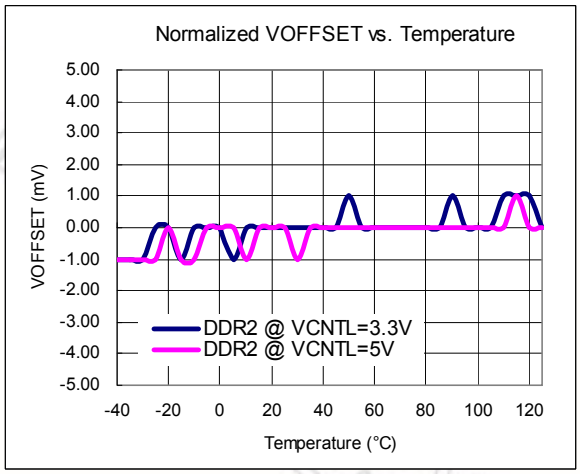

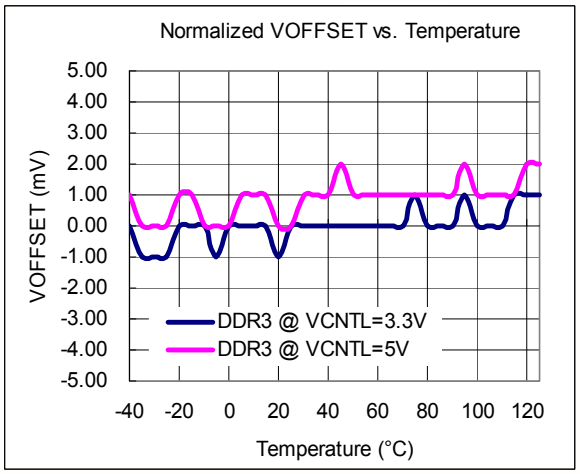

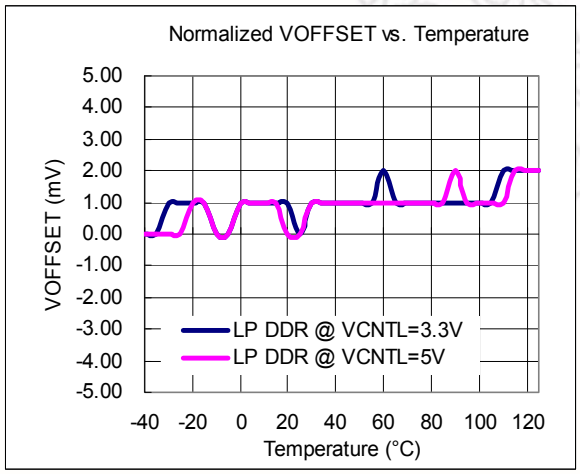

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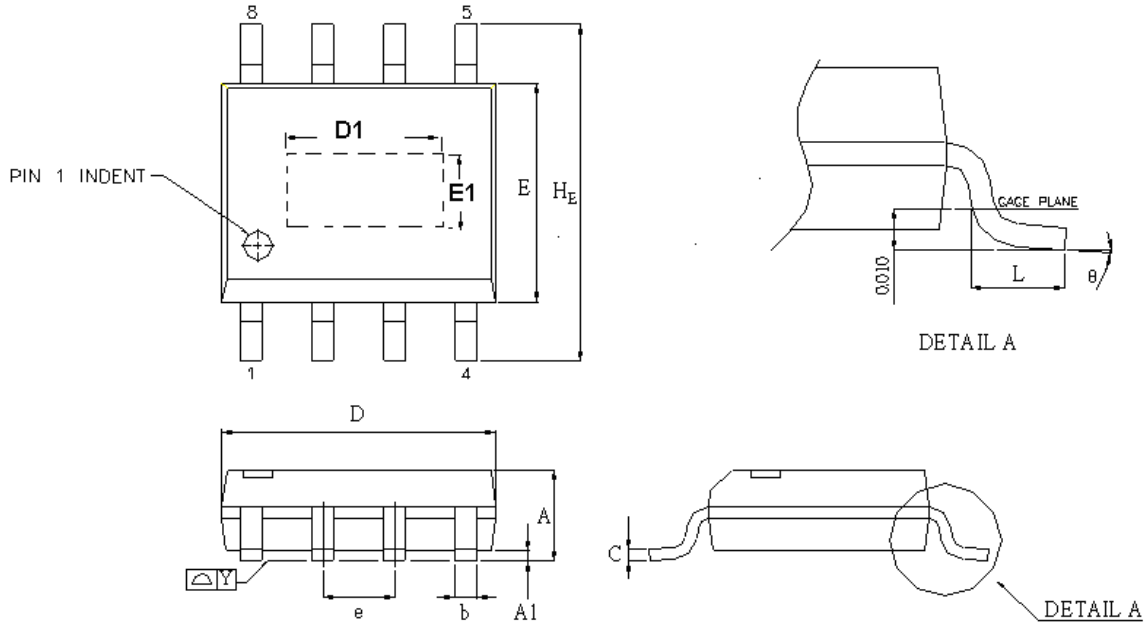
9. PACKAGE DIMENSION

SOP8-EP (150mil)

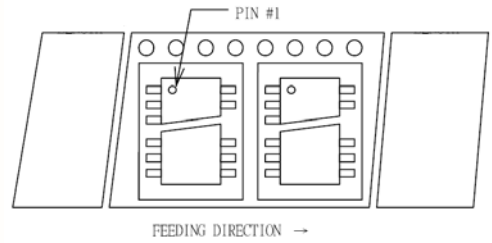


SYMBOLS	Dimensions In Millimeters		Dimensions In Inched	
	Min	Max	Min	Max
A	1.35	1.75	0.05	0.07
A1	0.05	0.25	0.00	0.01
b	0.31	0.51	0.01	0.02
c	0.10	0.25	0.00	0.01
D	4.70	5.10	0.19	0.20
E	3.80	4.00	0.15	0.16
e	1.27 BASIC		0.05 BASIC	
H_E	5.80	6.20	0.23	0.24
Y	--	0.10	--	0.00
L	0.40	1.27	0.02	0.05
θ	0°	10°	0°	10°
D1	Depend on L/F size			
E1	Depend on L/F size			

D1-1	1.94	2.29	0.08	0.09
D1-2	2.81	3.30	0.11	0.13
D1-3	3.10	3.50	0.12	0.14
E1-1	1.94	2.29	0.08	0.09
E1-2	2.05	2.41	0.08	0.09
E1-3	2.20	2.60	0.09	0.10

➢ **TAPING SPECIFICATION**

Note: W83312SN L/F size is D1-3 & E1-3 dimension



SOP8-EP Package

10. ORDERING INFORMATION

Part Number	Package Type	Supplied as	Production Flow
W83312SN	8PIN SOP8-EP (Green Package)	T Shape: 2,500 units/T&R	Commercial, -40°C to +85°C

11. TOP MARKING SPECIFICATION

1st Line: Nuvoton logo

2nd Line: W83312SN (Part number)

3rd line: Tracking code

- 752: packages assembled in Year 2007, week 52
- A: assembly house ID
- BB: Internal use only
- X: the IC version (A means A; B means B & C means C…etc.)

12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	11/28/2008	All	New Create
A2	12/29/2008	4, 5, 7	Update the linear regulator chart & VIN Recommended Range
A3	8/1/2009	All	1. Updated operating temperature range 2. Updated 6.2 General Regulator 3. Updated Typical Operating Waveforms
A4	1/29/2010	6	Correct Typo, add PCB Layout Suggestion
A5	3/31/2010	6,20	1. Add suggestion land pattern 2. Update the SOP8-EP package outline

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