

## Features

- Utilizes the ARM7TDMI® ARM® Thumb® Processor Core
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - Embedded ICE (In-circuit Emulation)
- 8K Bytes Internal SRAM
- Fully Programmable External Bus Interface (EBI)
  - Maximum External Address Space of 64M Bytes
  - Up to 8 Chip Selects
  - Software Programmable 8/16-bit External Data Bus
- 8-channel Peripheral Data Controller
- 8-level Priority, Individually Maskable, Vectored Interrupt Controller
  - 5 External Interrupts, Including a High-priority, Low-latency Interrupt Request
- 54 Programmable I/O Lines
- 6-channel 16-bit Timer/Counter
  - 6 External Clock Inputs, 2 Multi-purpose I/O Pins per Channel
- 2 USARTs
  - 2 Dedicated Peripheral Data Controller (PDC) Channels per USART
  - Support for up to 9-bit Data Transfers
- 2 Master/Slave SPI Interfaces
  - 2 Dedicated Peripheral Data Controller (PDC) Channels per SPI
  - 8- to 16-bit Programmable Data Length
  - 4 External Slave Chip Selects per SPI
- 3 System Timers:
  - Period Interval Timer (PIT); Real-time Timer (RTT); Watchdog Timer (WDT)
- Power Management Controller (PMC)
  - CPU and Peripherals Can be Deactivated Individually
- Clock Generator with 32.768 kHz Low-power Oscillator and PLL
  - Support for 38.4 kHz Crystals
  - Software Programmable System Clock (up to 33 MHz)
- IEEE® 1149.1 JTAG Boundary Scan on All Active Pins
- Fully Static Operation: 0 Hz to 33 MHz Internal Frequency Range at VDDCORE = 3.0V, 85° C
- 2.7V to 3.6V Core and PLL Operating Voltage Range; 2.7V to 5.5V I/O Operating Voltage Range
- -40° C to +85° C Temperature Range
- Available in a 144-lead LQFP Package (Green) and a 144-ball BGA Package (RoHS-compliant)

## 1. Description

The AT91M42800A is a member of the Atmel AT91 16/32-bit microcontroller family, which is based on the ARM7TDMI processor core. This processor has a high-performance 32-bit RISC architecture with a high-density 16-bit instruction set and very low power consumption. In addition, a large number of internally banked registers result in very fast exception handling, making the device ideal for real-time control applications. The AT91 ARM-based MCU family also features Atmel's high-density, in-system programmable, nonvolatile memory technology. The AT91M42800A has a direct connection to off-chip memory, including Flash, through the External Bus Interface.



## AT91 ARM Thumb Microcontrollers

### AT91M42800A

## Summary

Rev. 1779ES-ATARM-14-Apr-06



Note: This is a summary document. A complete document is available on our web site at [www.atmel.com](http://www.atmel.com).

The Power Management Controller allows the user to adjust device activity according to system requirements, and, with the 32.768 kHz low-power oscillator, enables the AT91M42800A to reduce power requirements to an absolute minimum. The AT91M42800A is manufactured using Atmel's high-density CMOS technology. By combining the ARM7TDMI processor core with on-chip SRAM and a wide range of peripheral functions including timers, serial communication controllers and a versatile clock generator on a monolithic chip, the AT91M42800A provides a highly-flexible and cost-effective solution to many compute-intensive applications.

## 2. Pin Configuration

Figure 2-1. Pin Configuration in LQFP144 Package (Top View)

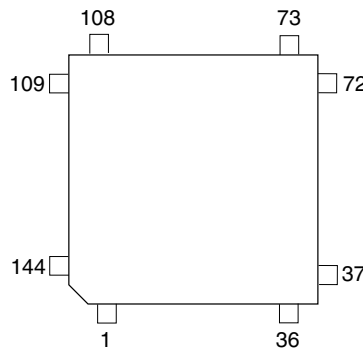
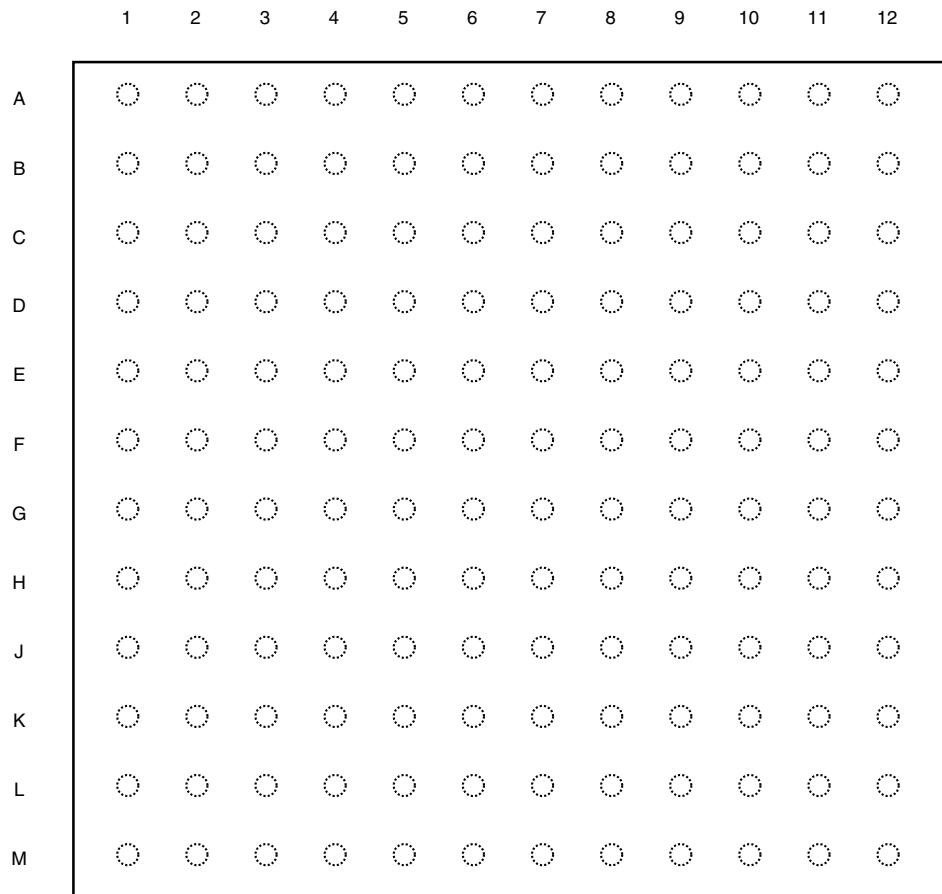


Figure 2-2. Pin Configuration in BGA144 Package (Top View)



**Table 2-1. AT91M42800A Pinout in LQFP 144 Package**

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	GND	37	GND	73	GND	109	GND
2	GND	38	GND	74	GND	110	GND
3	NLB/A0	39	D4	75	PB22/TIOA5	111	PA26
4	A1	40	D5	76	PB23/TIOB5	112	MODE0
5	A2	41	D6	77	PA0/IRQ0	113	XIN
6	A3	42	D7	78	PA1/IRQ1	114	XOUT
7	A4	43	D8	79	PA2/IRQ2	115	GND
8	A5	44	D9	80	PA3/IRQ3	116	PLLRC A
9	A6	45	D10	81	PA4/FIQ	117	VDDPLL
10	A7	46	D11	82	PA5/SCK0	118	PLLRCB
11	A8	47	D12	83	PA6/TXD0	119	VDDPLL
12	VDDIO	48	VDDIO	84	VDDIO	120	VDDIO
13	GND	49	GND	85	GND	121	GND
14	A9	50	D13	86	PA7/RXD0	122	NWDOVF
15	A10	51	D14	87	PA8/SCK1	123	PA27/BMS
16	A11	52	D15	88	PA9/TXD1/NTRI	124	MODE1
17	A12	53	PB6/TCLK0	89	PA10/RXD1	125	TMS
18	A13	54	PB7/TIOA0	90	PA11/SPCKA	126	TDI
19	A14	55	PB8/TIOB0	91	PA12/MISOA	127	TDO
20	A15	56	PB9/TCLK1	92	PA13/MOSIA	128	TCK
21	A16	57	PB10/TIOA1	93	PA14/NPCSA0/NSSA	129	NTRST
22	A17	58	PB11/TIOB1	94	PA15/NPCSA1	130	NRST
23	A18	59	PB12/TCLK2	95	PA16/NPCSA2	131	PA28
24	VDDIO	60	VDDIO	96	VDDIO	132	VDDIO
25	GND	61	GND	97	GND	133	GND
26	A19	62	PB13/TIOA2	98	PA17/NPCSA3	134	PA29/PME
27	PB2/A20/CS7	63	PB14/TIOB2	99	PA18/SPCKB	135	NWAIT
28	PB3/A21/CS6	64	PB15/TCLK3	100	PA19/MISOB	136	NOE/NRD
29	PB4/A22/CS5	65	PB16/TIOA3	101	PA20/MOSIB	137	NWE/NWR0
30	PB5/A23/CS4	66	PB17/TIOB3	102	PA21/NPCSB0/NSSB	138	NUB/NWR1
31	D0	67	PB18/TCLK4	103	PA22/NPCSB1	139	NCS0
32	D1	68	PB19/TIOA4	104	PA23/NPCSB2	140	NCS1
33	D2	69	PB20/TIOB4	105	PA24/NPCSB3	141	PB0/NCS2
34	D3	70	PB21/TCLK5	106	PA25/MCKO	142	PB1/NCS3
35	VDDCORE	71	VDDCORE	107	VDDCORE	143	VDDCORE
36	VDDIO	72	VDDIO	108	VDDIO	144	VDDIO

**Table 2-2.** AT91M42800A Pinout in BGA 144 Package

Pin#	Name
A1	PB1/NCS3
A2	NCS0
A3	NCS1
A4	GND
A5	PLLRCB
A6	GND
A7	PLLRCA
A8	GND
A9	XOUT
A10	XIN
A11	MODE0
A12	PA22/NPCSB1
B1	NUB/NWR1
B2	PB0/NCS2
B3	VDDCORE
B4	NWE/NWR0
B5	VDDPLL
B6	TDO
B7	VDDPLL
B8	NWDOVF
B9	PA26
B10	PA19/MISOB
B11	PA24/NPCSB3
B12	PA23/NPCSB2
C1	NLB/A0
C2	A1
C3	VDDIO
C4	NOE/NRD
C5	VDDIO
C6	NRST
C7	TDI
C8	VDDIO
C9	PA27/BMS
C10	VDDIO
C11	VDDCORE
C12	PA20/MOSIB

Pin#	Name
D1	A2
D2	A3
D3	A4
D4	NWAIT
D5	PA29/PME
D6	PA28
D7	TCK
D8	TMS
D9	MODE1
D10	PA25/MCKO
D11	PA21/NPCSB0
D12	PA18/SPCKB
E1	A7
E2	VDDIO
E3	A6
E4	A5
E5	GND
E6	GND
E7	GND
E8	NTRST
E9	PA13/MOSIA
E10	PA16/NPCSA2
E11	VDDIO
E12	PA17/NPCSA3
F1	A8
F2	A12
F3	A9
F4	A10
F5	GND
F6	GND
F7	GND
F8	GND
F9	PA12/MISOA
F10	PA15/NPCSA1
F11	PA11/SPCKA
F12	PA14/NPCSA0

Pin#	Name
G1	A17
G2	A16
G3	A11
G4	A13
G5	GND
G6	GND
G7	GND
G8	GND
G9	PA9/TXD1/NTRI
G10	PA10/RXD1
G11	PA8/SCK1
G12	PA7/RXD0
H1	A18
H2	VDDIO
H3	A15
H4	A14
H5	A19
H6	GND
H7	GND
H8	GND
H9	PA6/TXD0
H10	PA4/FIQ
H11	VDDIO
H12	PA5/SCK0
J1	PB5/A23/CS4
J2	D0
J3	PB4/A22/CS5
J4	PB3/A21/CS6
J5	PB2/A20/CS7
J6	D15
J7	PB6/TCLK0
J8	PB10/TIOA1
J9	PA3/IRQ3
J10	PA2/IRQ2
J11	PA0/IRQ0
J12	PA1/IRQ1

Pin#	Name
K1	D1
K2	VDDCORE
K3	VDDIO
K4	D9
K5	D10
K6	D14
K7	PB9/TCLK1
K8	PB13/TIOA2
K9	PB11/TIOB1
K10	VDDIO
K11	PB16/TIOA3
K12	PB23/TIOB5
L1	D3
L2	D2
L3	D5
L4	D8
L5	VDDIO
L6	D13
L7	PB8/TIOB0
L8	VDDIO
L9	PB17/TIOB3
L10	VDDCORE
L11	PB20/TIOB4
L12	PB22/TIOA5
M1	D4
M2	D6
M3	D7
M4	D11
M5	D12
M6	PB7/TIOA0
M7	PB12/TCLK2
M8	PB15/TCLK3
M9	PB14/TIOB2
M10	PB18/TCLK4
M11	PB19/TIOA4
M12	PB21/TCLK5

### 3. Pin Description

**Table 3-1.** AT91M42800A Pin Description

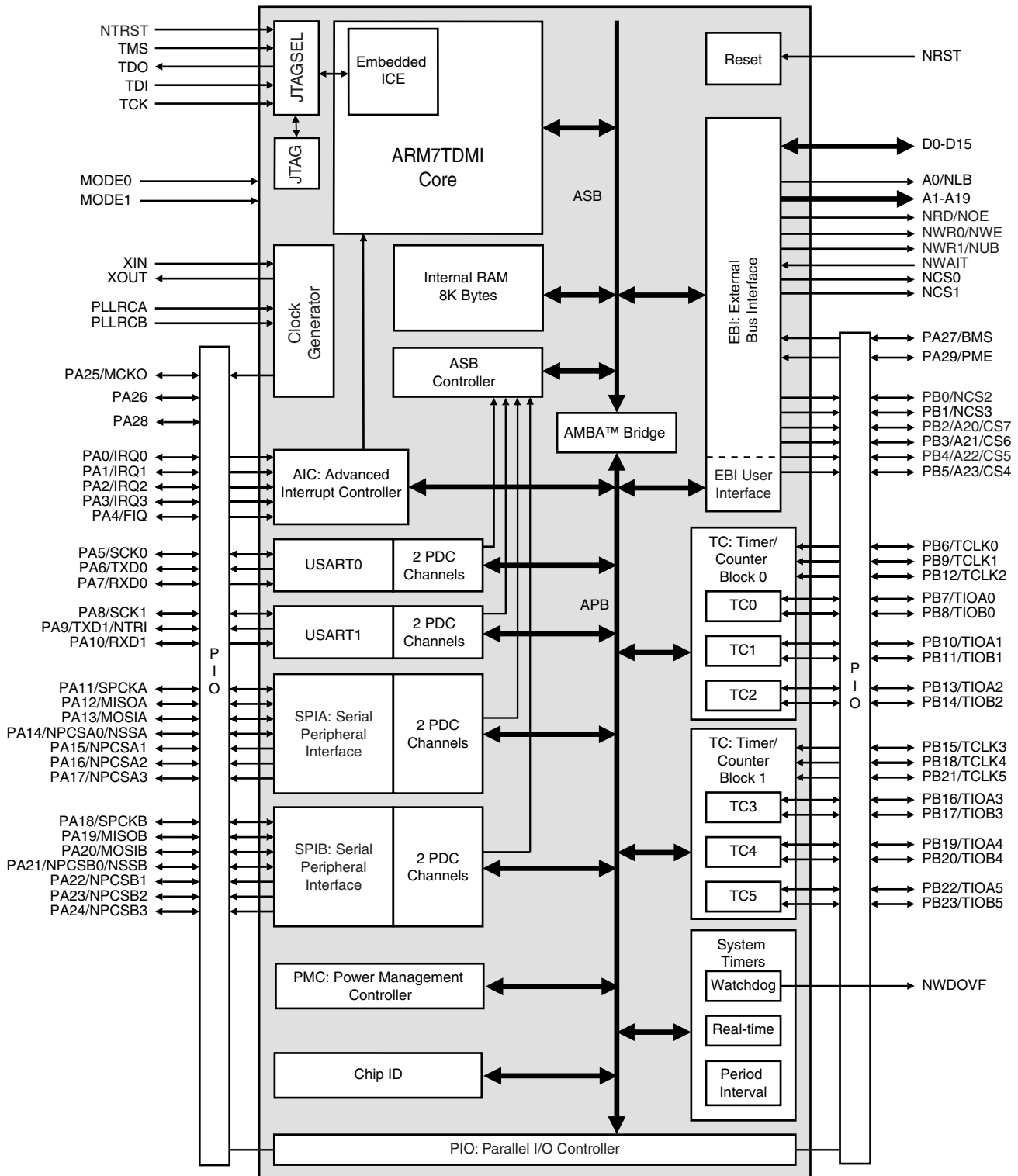
Module	Name	Function	Type	Active Level	Comments
EBI	A0 - A23	Address Bus	Output	–	All valid after reset
	D0 - D15	Data Bus	I/O	–	
	CS4 - CS7	Chip Select	Output	High	A23 - A20 after reset
	NCS0 - NCS3	Chip Select	Output	Low	
	NWR0	Lower Byte 0 Write Signal	Output	Low	Used in Byte Write option
	NWR1	Lower Byte 1 Write Signal	Output	Low	Used in Byte Write option
	NRD	Read Signal	Output	Low	Used in Byte Write option
	NWE	Write Enable	Output	Low	Used in Byte Select option
	NOE	Output Enable	Output	Low	Used in Byte Select option
	NUB	Upper Byte Select (16-bit SRAM)	Output	Low	Used in Byte Select option
	NLB	Lower Byte Select (16-bit SRAM)	Output	Low	Used in Byte Select option
	NWAIT	Wait Input	Input	Low	
	BMS	Boot Mode Select	Input	–	Sampled during reset
	PME	Protect Mode Enable	Input	High	PIO-controlled after reset
AIC	IRQ0 - IRQ3	External Interrupt Request	Input	–	PIO-controlled after reset
	FIQ	Fast External Interrupt Request	Input	–	PIO-controlled after reset
TC	TCLK0 - TCLK5	Timer External Clock	Input	–	PIO-controlled after reset
	TIOA0 - TIOA5	Multi-purpose Timer I/O Pin A	I/O	–	PIO-controlled after reset
	TIOB0 - TIOB5	Multi-purpose Timer I/O Pin B	I/O	–	PIO-controlled after reset
USART	SCK0 - SCK1	External Serial Clock	I/O	–	PIO-controlled after reset
	TXD0 - TXD1	Transmit Data Output	Output	–	PIO-controlled after reset
	RXD0 - RXD1	Receive Data Input	Input	–	PIO-controlled after reset
SPIA SPIB	SPCKA/SPCKB	Clock	I/O	–	PIO-controlled after reset
	MISOA/MISOB	Master In Slave Out	I/O	–	PIO-controlled after reset
	MOSIA/MOSIB	Master Out Slave In	I/O	–	PIO-controlled after reset
	NSSA/NSSB	Slave Select	Input	Low	PIO-controlled after reset
	NPCSA0 - NPCSA3 NPCSB0 - NPCSB3	Peripheral Chip Selects	Output	Low	PIO-controlled after reset
PIO	PA0 - PA29	Programmable I/O Port A	I/O	–	Input after reset
	PB0 - PB23	Programmable I/O Port B	I/O	–	Input after reset
ST	NWDOVF	Watchdog Timer Overflow	Output	Low	Open drain

**Table 3-1.** AT91M42800A Pin Description (Continued)

Module	Name	Function	Type	Active Level	Comments
CLOCK	XIN	Oscillator Input or External Clock	Input	–	
	XOUT	Oscillator Output	Output	–	
	PLLRCA	RC Filter for PLL A	Input	–	
	PLLRCB	RC Filter for PLL B	Input	–	
	MCKO	Clock Output	Output	–	
Test and Reset	NRST	Hardware Reset Input	Input	Low	Schmitt trigger
	MODE0 - MODE1	Mode Selection	Input	–	
JTAG/ICE	TMS	Test Mode Select	Input	–	Schmitt trigger, internal pull-up
	TDI	Test Data In	Input	–	Schmitt trigger, internal pull-up
	TDO	Test Data Out	Output	–	
	TCK	Test Clock	Input	–	Schmitt trigger, internal pull-up
	NTRST	Test Reset Input	Input	Low	Schmitt trigger, internal pull-up
Emulation	NTRI	Tri-state Mode Enable	Input	Low	Sampled during reset
Power	VDDIO	I/O Power	Power	–	3V or 5V nominal supply
	VDDCORE	Core Power	Power	–	3V nominal supply
	VDDPLL	PLL Power	Power	–	3V nominal supply
	GND	Ground	Ground	–	

## 4. Block Diagram

Figure 4-1. AT91M42800A





## 5. Architectural Overview

The AT91M42800A microcontroller integrates an ARM7TDMI with its embedded ICE interface, memories and peripherals. Its architecture consists of two main buses, the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB). Designed for maximum performance and controlled by the memory controller, the ASB interfaces the ARM7TDMI processor with the on-chip 32-bit memories, the External Bus Interface (EBI) and the AMBA™ Bridge. The AMBA Bridge drives the APB, which is designed for accesses to on-chip peripherals and optimized for low power consumption.

The AT91M42800A microcontroller implements the ICE port of the ARM7TDMI processor on dedicated pins, offering a complete, low-cost and easy-to-use debug solution for target debugging.

### 5.1 Memories

The AT91M42800A microcontroller embeds up to 8K bytes of internal SRAM. The internal memory is directly connected to the 32-bit data bus and is single-cycle accessible. This provides maximum performance of 30 MIPS at 33 MHz by using the ARM instruction set of the processor. The on-chip memory significantly reduces the system power consumption and improves its performance over external memory solutions.

The AT91M42800A microcontroller features an External Bus Interface (EBI), which enables connection of external memories and application-specific peripherals. The EBI supports 8- or 16-bit devices and can use two 8-bit devices to emulate a single 16-bit device. The EBI implements the early read protocol, enabling faster single clock cycle accesses two times faster than standard memory interfaces.

### 5.2 Peripherals

The AT91M42800A microcontroller integrates several peripherals, which are classified as system or user peripherals. All on-chip peripherals are 32-bit accessible by the AMBA Bridge, and can be programmed with a minimum number of instructions. The peripheral register set is composed of control, mode, data, status and enable/disable/status registers.

An on-chip Peripheral Data Controller (PDC) transfers data between the on-chip USARTs/SPIs and the on- and off-chip memories without processor intervention. Most importantly, the PDC removes the processor interrupt handling overhead and significantly reduces the number of clock cycles required for a data transfer. It can transfer up to 64K continuous bytes without reprogramming the start address. As a result, the performance of the microcontroller is increased and the power consumption reduced.

#### 5.2.1 System Peripherals

The External Bus Interface (EBI) controls the external memory and peripheral devices via an 8- or 16-bit data bus and is programmed through the APB. Each chip select line has its own programming register.

The Power Management Controller (PMC) optimizes power consumption of the product by controlling the clocking elements such as the oscillator and the two PLLs, system and user peripheral clocks.

The Advanced Interrupt Controller (AIC) controls the internal sources from the internal peripherals and the five external interrupt lines (including the FIQ) to provide an interrupt and/or fast



interrupt request to the ARM7TDMI. It integrates an 8-level priority controller, and, using the Auto-vectoring feature, reduces the interrupt latency time.

The Parallel Input/Output Controllers (PIOA, PIOB) controls up to 54 I/O lines. It enables the user to select specific pins for on-chip peripheral input/output functions, and general-purpose input/output signal pins. The PIO controllers can be programmed to detect an interrupt on a signal change from each line.

There are three embedded system timers. The Real-time Timer (RTT) counts elapsed seconds and can generate periodic or programmed interrupts. The Period Interval Timer (PIT) can be used as a user-programmable time-base, and can generate periodic ticks. The Watchdog (WD) can be used to prevent system lock-up if the software becomes trapped in a deadlock.

The Special Function (SF) module integrates the Chip ID and the Reset Status registers.

### 5.2.2 User Peripherals

Two USARTs, independently configurable, enable communication at a high baud rate in synchronous or asynchronous mode. The format includes start, stop and parity bits and up to 9 data bits. Each USART also features a Time-out and a Time-guard register, facilitating the use of the two dedicated Peripheral Data Controller (PDC) channels.

The two 3-channel, 16-bit Timer/Counters (TC) are highly-programmable and support capture or waveform modes. Each TC channel can be programmed to measure or generate different kinds of waves, and can detect and control two input/output signals. Each TC also has three external clock signals.

Two independently configurable SPIs provide communication with external devices in master or slave mode. Each has four external chip selects which can be connected to up to 15 devices. The data length is programmable, from 8- to 16-bit.

## 6. Associated Documentation

Table 6-1. Associated Documentation

Product	Information	Document Title
AT91M42800A	Internal architecture of processor ARM/Thumb instruction sets Embedded in-circuit-emulator	ARM7TDMI (Thumb) Datasheet
	External memory interface mapping Peripheral operations Peripheral user interfaces	AT91M42800A Datasheet
	DC characteristics Power consumption Thermal and reliability considerations AC characteristics	AT91M42800A Electrical Characteristics
	Product overview Ordering information Packaging information Soldering profile	AT91M42800A Summary Datasheet (this document)

## 7. Product Overview

### 7.1 Power Supply

The AT91M42800A has three kinds of power supply pins:

- VDDCORE pins, which power the chip core
- VDDIO pins, which power the I/O lines
- VDDPLL pins, which power the oscillator and PLL cells

VDDCORE and VDDIO pins allow core power consumption to be reduced by supplying it with a lower voltage than the I/O lines. The VDDCORE pins must never be powered at a voltage greater than the supply voltage applied to the VDDIO.

The VDDPLL pin is used to supply the oscillator and both PLLs. The voltage applied on these pins is typically 3.3V, and it must not be lower than VDDCORE.

Typical supported voltage combinations are shown in the following table:

Pins	Nominal Supply Voltages	
VDDCORE	3.3V	3.0V or 3.3V
VDDIO	5.0V	3.0V or 3.3V
VDDPLL	3.3V	3.0V or 3.3V

### 7.2 Input/Output Considerations

After the reset, the peripheral I/Os are initialized as inputs to provide the user with maximum flexibility. It is recommended that in any application phase, the inputs to the AT91M42800A microcontroller be held at valid logic levels to minimize the power consumption.

### 7.3 Operating Modes

The AT91M42800A has two pins dedicated to defining MODE0 and MODE1 operating modes. These pins allow the user to enter the device in Boundary Scan mode. They also allow the user to run the processor from the on-chip oscillator and from an external clock by bypassing the on-chip oscillator. The last mode is reserved for test purposes. A chip reset must be performed (NRST and NTRST) after MODE0 and/or MODE1 have been changed.

MODE0	MODE1	Operating Mode
0	0	Normal operating mode by using the on-chip oscillator
0	1	Boundary Scan Mode
1	0	Normal operating mode by using an external clock on XIN
1	1	Reserved for test

### 7.4 Clock Generator

The AT91M42800A microcontroller embeds a 32.768 kHz oscillator that generates the Slow Clock (SLCK). This on-chip oscillator can be bypassed by setting the correct logical level on MODE0 and MODE1 pins, as shown above. In this case, SLCK equals XIN.

The AT91M42800A microcontroller has a fully static design and works either on the Master Clock (MCK), generated from the Slow Clock by means of the two integrated PLLs, or on the Slow Clock (SLCK).

These clocks are also provided as an output of the device on the pin MCKO, which is multiplexed with a general-purpose I/O line. While NRST is active, and after the reset, the MCKO is valid and outputs an image of the SLCK signal. The PIO Controller must be programmed to use this pin as standard I/O line.

## 7.5 Reset

Reset initializes the user interface registers to their default states as defined in the peripheral sections of this datasheet and forces the ARM7TDMI to perform the next instruction fetch from address zero. Except for the program counter, the ARM core registers do not have defined reset states. When reset is active, the inputs of the AT91M42800A must be held at valid logic levels. The EBI address lines drive low during reset. All the peripheral clocks are disabled during reset to save power.

### 7.5.1 NRST Pin

NRST is the active low reset input. It is asserted asynchronously, but exit from reset is synchronized internally to the slow clock (SLCK). At power-up, NRST must be active until the on-chip oscillator is stable. During normal operation, NRST must be active for a minimum of 10 SLCK clock cycles to ensure correct initialization.

The pins BMS and NTRI are sampled during the 10 SLCK clock cycles just prior to the rising edge of NRST.

The NRST pin has no effect on the on-chip Embedded ICE logic.

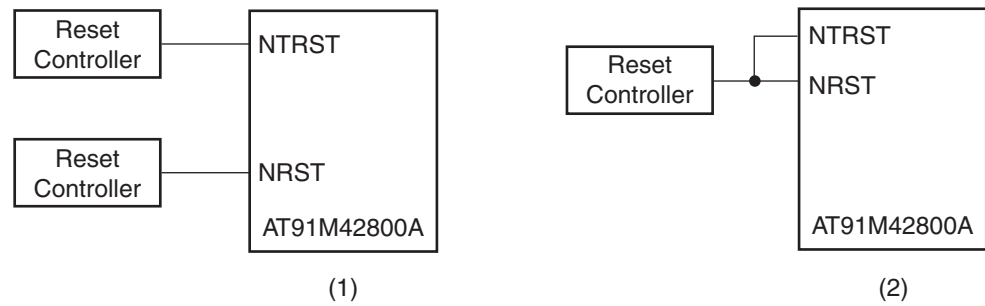
Test Access Port (TAP) reset functionality is provided through the NTRST signal.

### 7.5.2 NTRST Pin

The NTRST control pin initializes the selected TAP controller. The TAP controller involved in this reset is determined according to the initial logical state applied on the JTAGSEL pin after the last valid NRST.

In either Boundary Scan or ICE Mode, a reset can be performed from the same or different circuitry, as shown in [Figure 7-1 on page 13](#) below. But in all cases, the NTRST like the NRST signal, must be asserted after each power-up. (See the AT91M42800A Electrical Datasheet, Atmel Lit. No. 1776, for the necessary minimum pulse assertion time.)

**Figure 7-1.** Separate or Common Reset Management



- Notes: 1. NRST and NTRST handling in Debug Mode during development.  
2. NRST and NTRST handling during production.

In order to benefit from the separation of NRST and NTRST during the debug phase of development, the user must independently manage both signals as shown in example (1) of Figure 7-1 above. However, once debug is completed, both signals are easily managed together during production as shown in example (2) of Figure 7-1 above.

### 7.5.3 Watchdog Reset

The internally generated watchdog reset has the same effect as the NRST pin, except that the pins BMS and NTRI are not sampled. Boot mode and Tri-state mode are not updated. The NRST pin has priority if both types of reset coincide.

## 7.6 Emulation Functions

### 7.6.1 Tri-state Mode

The AT91M42800A provides a Tri-state mode, which is used for debug purposes in order to connect an emulator probe to an application board. In Tri-state mode the AT91M42800A continues to function, but all the output pin drivers are tri-stated.

To enter Tri-state mode, the pin NTRI must be held low during the last 10 SLCK clock cycles before the rising edge of NRST. For normal operation, the pin NTRI must be held high during reset, by a resistor of up to 400 kΩ. NTRI must be driven to a valid logic value during reset.

NTRI is multiplexed with Parallel I/O PA9 and USART 1 serial data transmit line TXD1.

Standard RS232 drivers generally contain internal 400 kΩ pull-up resistors. If TXD1 is connected to one of these drivers, this pull-up will ensure normal operation, without the need for an additional external resistor.

### 7.6.2 Embedded ICE

ARM standard embedded in-circuit emulation is supported via the JTAG/ICE port. It is connected to a host computer via an embedded ICE Interface.

Embedded ICE mode is selected when MODE1 is low.

It is not possible to switch directly between ICE and JTAG operations. A chip reset must be performed (NRST and NTRST) after MODE0 and/or MODE1 have/has been changed. The reset input to the Embedded ICE (NTRST) is provided separately to facilitate debug of boot programs.

### 7.6.3 IEEE 1149.1 JTAG Boundary Scan

IEEE 1149.1 JTAG Boundary Scan is enabled when MODE0 is low and MODE1 is high. The functions SAMPLE, EXTEST and BYPASS are implemented. In ICE Debug mode, the ARM core responds with a non-JTAG chip ID that identifies the core to the ICE system. This is not IEEE 1149.1 JTAG compliant. It is not possible to switch directly between JTAG and ICE operations. A chip reset must be performed (NRST and NTRST) after MODE0 and MODE1 are changed.

## 7.7 Memory Controller

The ARM7TDMI processor address space is 4G bytes. The memory controller decodes the internal 32-bit address bus and defines three address spaces:

- Internal Memories in the four lowest megabytes
- Middle Space reserved for the external devices (memory or peripherals) controlled by the EBI
- Internal Peripherals in the four highest megabytes

In any of these address spaces, the ARM7TDMI operates in little-endian mode only.

### 7.7.1 Protection Mode

The embedded peripherals can be protected against unwanted access. The PME (Protect Mode Enable) pin must be tied high and validated in its peripheral operation (PIO Disable) to enable the protection mode. When enabled, any peripheral access must be done while the ARM7TDMI is running in Privileged mode (i.e., the accesses in user mode result in an abort). Only the valid peripheral address space is protected and requests to the undefined addresses will lead to a normal operation without abort.

### 7.7.2 Internal Memories

The AT91M42800A microcontroller integrates an 8-Kbyte primary internal SRAM. All internal memories are 32 bits wide and single-clock cycle accessible. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one cycle. Fetching Thumb or ARM instructions is supported and internal memory can store twice as many Thumb instructions as ARM ones.

The SRAM bank is mapped at address 0x0 (after the remap command), and ARM7TDMI exception vectors between 0x0 and 0x20 that can be modified by the software. The rest of the bank can be used for stack allocation (to speed up context saving and restoring), or as data and program storage for critical algorithms.

### 7.7.3 Boot Mode Select

The ARM reset vector is at address 0x0. After the NRST line is released, the ARM7TDMI executes the instruction stored at this address. This means that this address must be mapped in nonvolatile memory after the reset.

The input level on the BMS pin during the last 10 SLCK clock cycles before the rising edge of the NRST selects the type of boot memory. The Boot mode depends on BMS (see Table 7-1).

The pin BMS is multiplexed with the I/O line PA27 that can be programmed after reset like any standard PIO line.

**Table 7-1.** Boot Mode Select

BMS	Boot Memory
1	External 8-bit memory NCS0
0	External 16-bit memory on NCS0

## 7.7.4 Remap Command

The ARM vectors (Reset, Abort, Data Abort, Prefetch Abort, Undefined Instruction, Interrupt, Fast Interrupt) are mapped from address 0x0 to address 0x20. In order to allow these vectors to be redefined dynamically by the software, the AT91M42800A microcontroller uses a remap command that enables switching between the boot memory and the internal SRAM bank addresses. The remap command is accessible through the EBI User Interface, by writing one in RCB of EBI\_RCR (Remap Control Register). Performing a remap command is mandatory if access to the other external devices (connected to chip selects 1 to 7) is required. The remap operation can only be changed back by an internal reset or an NRST assertion.

## 7.7.5 Abort Control

The abort signal providing a Data Abort or a Prefetch Abort exception to the ARM7TDMI is asserted in the following cases:

- When accessing an undefined address in the EBI address space
- When the ARM7TDMI performs a misaligned access

No abort is generated when reading the internal memory or by accessing the internal peripherals, whether the address is defined or not.

When the processor performs a forbidden write access in a mode-protected peripheral register, the write is cancelled but no abort is generated.

The processor can perform word or half-word data access with a misaligned address when a register relative load/store instruction is executed and the register contains a misaligned address. In this case, whether the access is in write or in read, an abort is generated but the access is not cancelled.

The Abort Status Register traces the source that caused the last abort. The address and the type of abort are stored in registers of the External Bus Interface.

## 7.7.6 External Bus Interface

The External Bus Interface handles the accesses between addresses 0x0040 0000 and 0xFFC0 0000. It generates the signals that control access to the external devices, and can be configured from eight 1-Mbyte banks up to four 16-Mbyte banks. In all cases it supports byte, half-word and word aligned accesses.

For each of these banks, the user can program:

- Number of wait states
- Number of data float times (wait time after the access is finished to prevent any bus contention in case the device takes too long in releasing the bus)
- Data bus width (8-bit or 16-bit)

- With a 16-bit wide data bus, the user can program the EBI to control one 16-bit device (Byte Access Select mode) or two 8-bit devices in parallel that emulate a 16-bit memory (Byte Write Access mode).

The External Bus Interface also features the Early Read Protocol, configurable for all the devices, which significantly reduces access time requirements on an external device.

## 8. Peripherals

The AT91M42800A peripherals are connected to the 32-bit wide Advanced Peripheral Bus. Peripheral registers are only word accessible. Byte and half-word accesses are not supported. If a byte or a half-word access is attempted, the memory controller automatically masks the lowest address bits and generates a word access.

Each peripheral has a 16-Kbyte address space allocated (the AIC only has a 4-Kbyte address space).

### 8.1 Peripheral Registers

The following registers are common to all peripherals:

- Control Register – Write-only register that triggers a command when a one is written to the corresponding position at the appropriate address. Writing a zero has no effect.
- Mode Register – read/write register that defines the configuration of the peripheral. Usually has a value of 0x0 after a reset.
- Data Registers – read and/or write register that enables the exchange of data between the processor and the peripheral.
- Status Register – Read-only register that returns the status of the peripheral.
- Enable/Disable/Status Registers – shadow command registers. Writing a one in the Enable Register sets the corresponding bit in the Status Register. Writing a one in the Disable Register resets the corresponding bit and the result can be read in the Status Register. Writing a bit to zero has no effect. This register access method maximizes the efficiency of bit manipulation, and enables modification of a register with a single non-interruptible instruction, replacing the costly read-modify-write operation.

Unused bits in the peripheral registers are shown as “–” and must be written at 0 for upward compatibility. These bits read 0.

### 8.2 Peripheral Interrupt Control

The Interrupt Control of each peripheral is controlled from the status register using the interrupt mask. The status register bits are ANDed to their corresponding interrupt mask bits and the result is then ORed to generate the Interrupt Source signal to the Advanced Interrupt Controller.

The interrupt mask is read in the Interrupt Mask Register and is modified with the Interrupt Enable Register and the Interrupt Disable Register. The enable/disable/status (or mask) makes it possible to enable or disable peripheral interrupt sources with a non-interruptible single instruction. This eliminates the need for interrupt masking at the AIC or Core level in real-time and multi-tasking systems.



### 8.3 Peripheral Data Controller

The AT91M42800A has an 8-channel PDC dedicated to the two on-chip USARTs and to the two on-chip SPIs. One PDC channel is connected to the receiving channel and one to the transmitting channel of each peripheral.

The user interface of a PDC channel is integrated in the memory space of each USART channel and in the memory space of each SPI. It contains a 32-bit address pointer register and a 16-bit count register. When the programmed data is transferred, an end-of-transfer interrupt is generated by the corresponding peripheral. See the USART section and the SPI sections for more details on PDC operation and programming.

## 8.4 System Peripherals

### 8.4.1 PMC: Power Management Controller

The AT91M42800A's Power Management Controller optimizes the power consumption of the device. The PMC controls the clocking elements such as the oscillator and the PLLs, and the System and the Peripheral Clocks. It also controls the MCKO pin and permits to the user to select four different signals to be driven on this pin.

The AT91M42800A has the following clock elements:

- The oscillator providing a clock that depends on the crystal fundamental frequency connected between the XIN and XOUT pins
- PLL A providing a low-to-middle frequency clock range
- PLL B providing a middle-to-high frequency range
- The Clock prescaler
- The ARM Processor Clock controller
- The Peripheral Clock controller
- The Master Clock Output controller

The on-chip low-power oscillator together with the PLL-based frequency multiplier and the prescaler results in a programmable clock between 500 Hz and 66 MHz. It is the responsibility of the user to make sure that the PMC programming does not result in a clock over the acceptable limits.

### 8.4.2 ST: System Timer

The System Timer module integrates three different free-running timers:

- A Period Interval Timer setting the base time for an Operating System.
- A Watchdog Timer that is built around a 16-bit counter, and is used to prevent system lock-up if the software becomes trapped in a deadlock. It can generate an internal reset or interrupt, or assert an active level on the dedicated pin NWDOVF.
- A Real-time Timer counting elapsed seconds.

These timers count using the Slow Clock provided by the MCU. Typically, this clock has a frequency of 32768 Hz.

### 8.4.3 AIC: Advanced Interrupt Controller

The AT91M42800A has an 8-level priority, individually maskable, vectored interrupt controller. This feature substantially reduces the software and real-time overhead in handling internal and external interrupts.

The interrupt controller is connected to the NFIQ (fast interrupt request) and the NIRQ (standard interrupt request) inputs of the ARM7TDMI processor. The processor's NFIQ line can only be asserted by the external fast interrupt request input: FIQ. The NIRQ line can be asserted by the interrupts generated by the on-chip peripherals and the external interrupt request lines: IRQ0 to IRQ3.

The 8-level priority encoder allows the customer to define the priority between the different NIRQ interrupt sources.

Internal sources are programmed to be level sensitive or edge triggered. External sources can be programmed to be positive or negative edge triggered or high- or low-level sensitive.

#### **8.4.4 PIO: Parallel I/O Controller**

The AT91M42800A has 54 programmable I/O lines. I/O lines are multiplexed with an external signal of a peripheral to optimize the use of available package pins. These lines are controlled by two separate and identical PIO Controllers called PIOA and PIOB. Each PIO controller also provides an internal interrupt signal to the Advanced Interrupt Controller and insertion of a simple input glitch filter on any of the PIO pins.

#### **8.4.5 SF: Special Function**

The AT91M42800A provides registers that implement the following special functions.

- Chip Identification
- RESET Status

### **8.5 User Peripherals**

#### **8.5.1 USART: Universal Synchronous/Asynchronous Receiver Transmitter**

The AT91M42800A provides two identical, full-duplex, universal synchronous/asynchronous receiver/transmitters that interface to the APB and are connected to the Peripheral Data Controller.

The main features are:

- Programmable Baud Rate Generator with External or Internal Clock, as well as Slow Clock
- Parity, Framing and Overrun Error Detection
- Line Break Generation and Detection
- Automatic Echo, Local Loopback and Remote Loopback channel modes
- Multi-drop mode: Address Detection and Generation
- Interrupt Generation
- Two Dedicated Peripheral Data Controller channels
- 5-, 6-, 7-, 8- and 9-bit character length

#### **8.5.2 TC: Timer/Counter**

The AT91M42800A features two Timer/Counter blocks, each containing three identical 16-bit Timer/Counter channels. Each channel can be independently programmed to perform a wide range of functions including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse-width modulation.

Each Timer/Counter (TC) channel has 3 external clock inputs, 5 internal clock inputs, and 2 multi-purpose input/output signals that can be configured by the user. Each channel drives an

internal interrupt signal that can be programmed to generate processor interrupts via the AIC (Advanced Interrupt Controller).

The Timer/Counter block has two global registers that act upon all three TC channels. The Block Control Register allows the three channels to be started simultaneously with the same instruction. The Block Mode Register defines the external clock inputs for each Timer/Counter channel, allowing them to be chained.

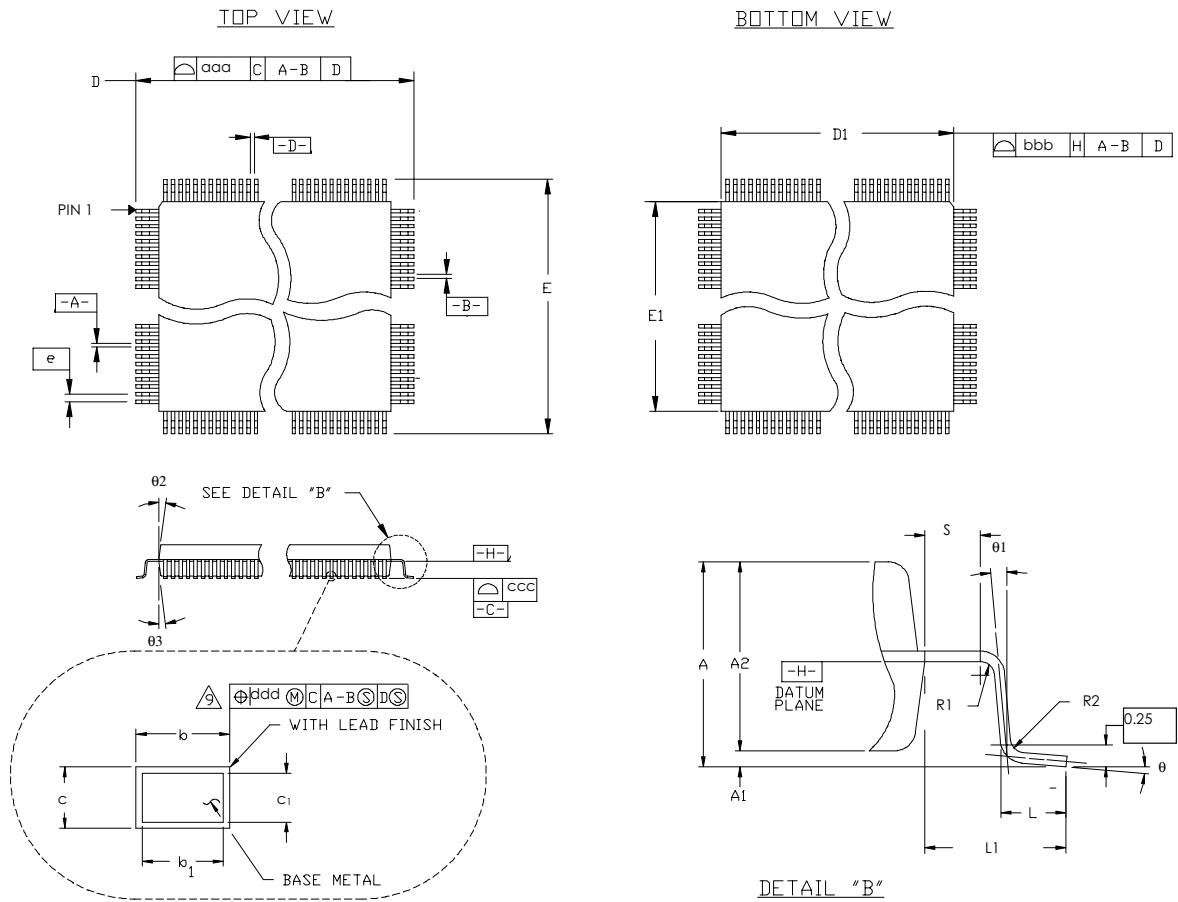
Each Timer/Counter block operates independently and has a complete set of block and channel registers.

### **8.5.3 SPI: Serial Peripheral Interface**

The AT91M42800A includes two SPIs that provide communication with external devices in Master or Slave mode. They are independent, and are referred to by the letters A and B. Each SPI has four external chip selects that can be connected to up to 15 devices. The data length is programmable from 8- to 16-bit.

## 9. Packaging Information

Figure 9-1. 144-lead LQFP Package Drawing



**Table 9-1.** Common Dimensions (mm)

Symbol	Min	Nom	Max
c	0.09		0.2
c1	0.09		0.16
L	0.45	0.6	0.75
L1	1.00 REF		
R2	0.08		0.2
R1	0.08		
S	0.2		
q	0°	3.5°	7°
q1	0°		
q2	11°	12°	13°
q3	11°	12°	13°
A			1.6
A1	0.05		0.15
A2	1.35	1.4	1.45
<b>Tolerances and form of position</b>			
aaa		0.2	
bbb		0.2	

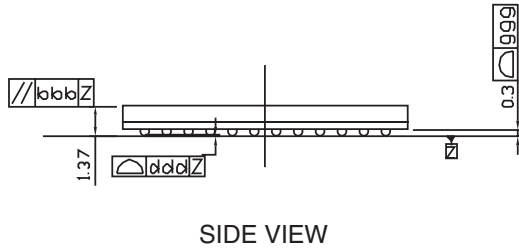
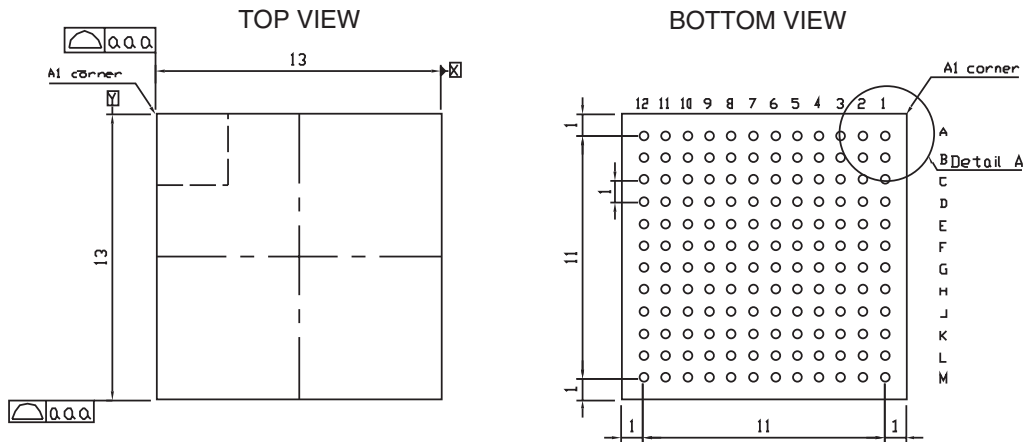
**Table 9-2.** Lead Count Dimensions (mm)

Pin Count	D/E BSC	D1/E1 BSC	b			b1			e BSC	ccc	ddd
			Min	Nom	Max	Min	Nom	Max			
144	22.0	20.0	0.17	0.22	0.27	0.17	0.2	0.23	0.50	0.10	0.08

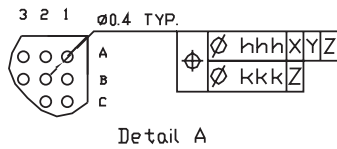
**Table 9-3.** Device and 144-lead LQFP Package Maximum Weight

1708	mg
------	----

**Figure 9-2.** 144-ball Ball Grid Array Package Drawing



Symbol	Max.
aaa	0.1
bbb	0.3
ddd	0.15
ggg	0.03
hhh	0.1
kkk	0.1



NOTES

1. Package dimensions conform to JESD-95-1 Section 5
2. Dimensioning and tolerancing per ASME Y14.5M-1994
3. All dimensions in mm
4. Solder Ball position designation per JESD 95-1, SPP-010
5. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls

**Table 9-4.** Device and 144-ball BGA Package Maximum Weight

584	mg
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## 10. Soldering Profile

### 10.1 LQFP Soldering Profile (Green)

Table 10-1 gives the recommended soldering profile from J-STD-020C.

**Table 10-1.** Soldering Profile Green Compliant Package

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3° C/sec. max.
Preheat Temperature 175°C ±25°C	180 sec. max.
Temperature Maintained Above 217°C	60 sec. to 150 sec.
Time within 5° C of Actual Peak Temperature	20 sec. to 40 sec.
Peak Temperature Range	260° C
Ramp-down Rate	6° C/sec. max.
Time 25° C to Peak Temperature	8 min. max.

Note: The package is certified to be backward compatible with Pb/Sn soldering profile.

A maximum of three reflow passes is allowed per component.

### 10.2 BGA Soldering Profile (RoHS-compliant)

Table 10-2 gives the recommended soldering profile from J-STD-20C.

**Table 10-2.** Soldering Profile RoHS Compliant Package

Profile Feature	Convection or IR/Convection
Average Ramp-up Rate (183° C to Peak)	3° C/sec. max.
Preheat Temperature 125° C ±25° C	180 sec. max
Temperature Maintained Above 183° C	60 sec. to 150 sec.
Time within 5° C of Actual Peak Temperature	20 sec. to 40 sec.
Peak Temperature Range	260° C
Ramp-down Rate	6° C/sec.
Time 25° C to Peak Temperature	8 min. max

Note: It is recommended to apply a soldering temperature higher than 250°C.

A maximum of three reflow passes is allowed per component.



## 11. Ordering Information

**Table 11-1.** Ordering Information

Ordering Code	Package	Package Type	Operating Temperature Range
AT91M42800A-33CJ	BGA 144	RoHS-compliant	Industrial (-40° C to 85° C)
AT91M42800A-33AU	LQFP 144	Green	





## 12. Revision History

Table 12-1. Revision History

Version	Comments	Change Request Ref.
1779AS	First issue Oct-01	
1779BS	Added information to section Internal Memories on page 13.	
	Change in Table 6 on page 19.	
	Added Table 9 on page 21.	
	Added Table 10 on page 22.	
1779CS	Added section Soldering Profile on page 23.	
	Updated package name to LQFP throughout.	
1779DS	Updated "Ordering Information" on page 24 and "Soldering Profile" on page 23 with new data on Green/RoHS-compliant packages.	05-329
1779ES	Added Section 7.5.2 "NTRST Pin" on page 12.	05-474
1779ES	Updated Section 10. "Soldering Profile" on page 23 and Section 11. "Ordering Information" on page 24 to remove leaded package references.	





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