Stepping Motor Drivers

Standard 36V Stepping Motor Driver

BD6290EFV

No.12009EAT03

●Description

BD6290EFV is the simple type that provides the minimum function for driving stepping motor and various protection circuits. As for its basic function, it is a low power consumption bipolar PWM constant current-drive driver with power supply's rated voltage of 36V and rated output current of 0.8A. There are excitation modes of FULL STEP & HALF STEP &, QUARTER STEP mode. This IC contributes to reduction of mounting area, cost down, safety design.

●Feature

1) Power supply: one system drive (rated voltage of 36V)
2) Rated output current: 0.8A
3) Low ON resistance DMOS output
4) Parallel IN drive mode
5) PWM constant current control (self oscillation)
6) Built-in spike noise cancel function (external noise filter is unnecessary)
7) FULL STEP, HALF STEP, QUARTER STEP
8) Power save function
9) Built-in logic input pull-down resistor
10) Power-on reset function
11) Thermal shutdown circuit (TSD)
12) Over current protection circuit (OCP)
13) Under voltage lock out circuit (UVLO)
14) Over voltage lock out circuit (OVLO)
15) Malfunction prevention at the time of no applied power supply (Ghost Supply Prevention Function)
16) Electrostatic discharge: 4kV (HBM specification)
17) Microminiature, ultra-thin and high heat-radiation (exposed metal type) HTSSOP package (BD6391EFV)

●Application

Laser beam printer, Scanner, Photo printer, FAX, Ink jet printer, Mini printer, Sewing machine, Toy, and Robot etc.

●Absolute maximum ratings(Ta=25℃)

Item	Symbol	Limit	Unit
Supply voltage	$V_{M1,2}$	-0.2～+36.0	V
Power dissipation	Pd	1.10※1	W
		4.00※2	
Input voltage for control pin	V_{IN}	-0.2～+7.0	V
RNF maximum voltage	V_{RNF}	0.5	V
Maximum output current	I_{OUT}	0.8※3	A/phase
Operating temperature range	T_{opr}	-25～+85	℃
Storage temperature range	T_{stg}	-55～+150	℃
Junction temperature	T_{jmax}	150	℃

※1 70mm×70mm×1.6mm glass epoxy board. Derating in done at 8.8mW/℃ for operating above Ta=25℃.
※2 4-layer recommended board. Derating in done at 32.0mW/℃ for operating above Ta=25℃.
※3 Do not, however exceed Pd, ASO and T_{jmax}=150℃.

●Operating conditions(Ta= -25～+85℃)

Item	Symbol	Limit	Unit
Supply voltage	$V_{M1,2}$	19～28	V
Output current (DC)	I_{OUT}	0.5※4	A/phase

※4 Do not however exceed Pd, ASO.

●Electrical characteristics

(Unless otherwise specified Ta=25℃, V_M=24V)

Item	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Whole						
Circuit current at standby	I_{VMST}	-	0.6	1.5	mA	PS=L
Circuit current	I_{VM}	-	3.0	7.0	mA	PS=H, VREF=2V
Control input (PHA1, I01, I11, PHA2, I02, I12, P.S.)						
H level input voltage	V_{PSH}	2.0	-	5.5	V	
L level input voltage	V_{PSL}	-	-	0.8	V	
H level input current	I_{PSH}	25	50	80	μA	Control input voltage=5V
L level input current	I_{PSL}	-	0	10	μA	Control input voltage=0V
Output (OUT1A, OUT1B, OUT2A, OUT2B)						
Output ON resistance	R_{ON}	-	2.80	3.60	Ω	I_{OUT} =±0.3A Sum of upper and lower
Output leak current	I_{LEAK}	-	-	10	μA	
Current control						
RNFX input current	I_{RNFX}	-40	-20	-	μA	RNFX=0V
VREF input current	I_{VREF}	-2.0	-0.1	-	μA	VREF=0V
VREF input voltage range	V_{REF}	0	-	2	V	
Comparator threshold 100%	V_{CTHLL}	0.340	0.400	0.460	V	VREF=2V,I0X=L,I1X=L
Comparator threshold 67%	V_{CTHHL}	0.227	0.267	0.307	V	VREF=2V,I0X=H,I1X=L
Comparator threshold 33%	V_{CTHLH}	0.113	0.133	0.153	V	VREF=2V,I0X=L,I1X=H
Minimum on time	t_{ONMIN}	0.3	0.5	1.0	μs	R=39kΩ, C=1000pF

●Terminal function・Block diagram・Application circuit diagram

Pin No.	Pin name	Function	Pin No.	Pin name	Function
1	PHA1	Logic input terminal	13	I02	Logic input terminal for DAC
2	PGND	Ground terminal	14	I12	Logic input terminal for DAC
3	VM1	Power supply terminal	15	NC	Non connection
4	OUT1A	H bridge output terminal	16	CR2	Connection terminal of CR for setting PWM frequency
5	RNF1	Connection terminal of resistor for output current detection	17	TEST	Terminal for testing (used by connecting with GND)
6	OUT1B	H bridge output terminal	18	NC	Non connection
7	OUT2B	H bridge output terminal	19	GND	Ground terminal
8	RNF2	Connection terminal of resistor for output current detection	20	PS	Power save terminal
9	OUT2A	H bridge output terminal	21	CR1	Connection terminal of CR for setting PWM frequency
10	VM2	Power supply terminal	22	VREF	Output current value setting terminal
11	NC	Non connection	23	I11	Logic input terminal for DAC
12	PHA2	Logic input terminal	24	I01	Logic input terminal for DAC

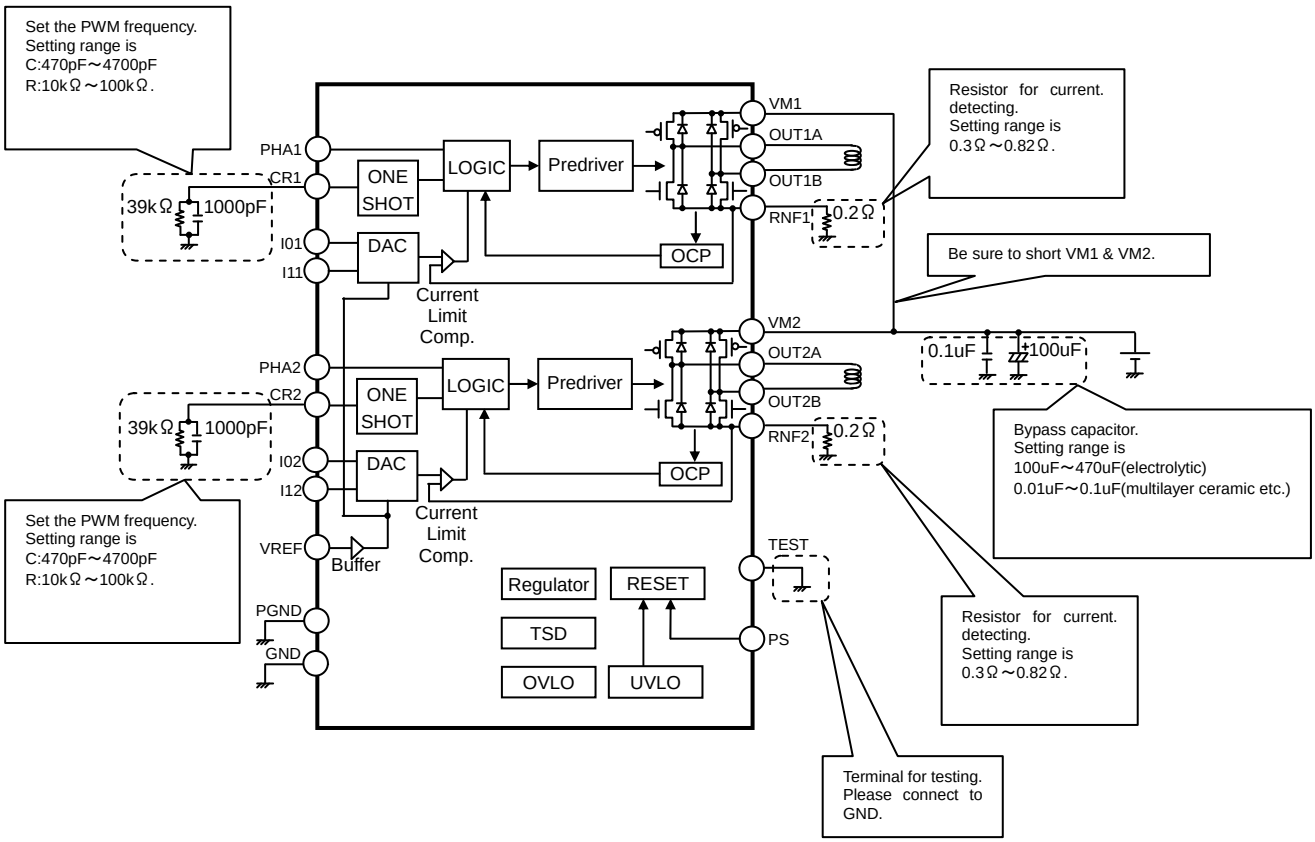


Fig.1 Block diagram & Application circuit diagram

●Points to notice for terminal description

○PS／Power save terminal

PS can make circuit standby state and make motor output OPEN. Please be careful because there is a delay of 40μs(max.) before it is returned from standby state to normal state and the motor output becomes ACTIVE.

PS	State
L	Standby state (RESET)
H	ACTIVE

○PHA1,PHA2／Logic input terminal

These terminals decide output state.

PHAX	OUTXA	OUTXB
L	L	H
H	H	L

○I01,I02,I11,I12／Logic input terminal for DAC

These terminals decide internal DAC output voltage for current limit.

I0X	I1X	Output current level(%)
L	L	100
H	L	67
L	H	33
H	H	0

(I0X,I1X)=(H,H) : motor output are open.

●Protection Circuits

○Thermal Shutdown (TSD)

This IC has a built-in thermal shutdown circuit for thermal protection. When the IC's chip temperature rises above 175℃ (Typ.), the motor output becomes OPEN. Also, when the temperature returns to under 150℃ (Typ.), it automatically returns to normal operation. However, even when TSD is in operation, if heat is continued to be added externally, heat overdrive can lead to destruction.

○Over Current Protection (OCP)

This IC has a built in over current protection circuit as a provision against destruction when the motor outputs are shorted each other or V_M－motor output or motor output－GND is shorted. This circuit latches the motor output to OPEN condition when the regulated threshold current flows for 4μs (Typ.). It returns with power reactivation or a reset of the PS terminal. The over current protection circuit's only aim is to prevent the destruction of the IC from irregular situations such as motor output shorts, and is not meant to be used as protection or security for the set. Therefore, sets should not be designed to take into account this circuit's functions. After OCP operating, if irregular situations continue and the return by power reactivation or a reset of the PS terminal is carried out repeatedly, then OCP operates repeatedly and the IC may generate heat or otherwise deteriorate. When the L value of the wiring is great due to the wiring being long, after the over current has flowed and the output terminal voltage jumps up and the absolute maximum values may be exceeded and as a result, there is a possibility of destruction. Also, when current which is over the output current rating and under the OCP detection current flows, the IC can heat up to over T_{jmax} =150℃ and can deteriorate, so current which exceeds the output rating should not be applied.

○Under Voltage Lock Out (UVLO)

This IC has a built-in under voltage lock out function to prevent false operation such as IC output during power supply under voltage. When the applied voltage to the V_M terminal goes under 15V (Typ.), the motor output is set to OPEN. This switching voltage has a 1V (Typ.) hysteresis to prevent false operation by noise etc. Please be aware that this circuit does not operate during power save mode.

○Over Voltage Lock Out (OVLO)

This IC has a built-in over voltage lock out function to protect the IC output and the motor during power supply over voltage. When the applied voltage to the VM terminal goes over 32V (Typ.), the motor output is set to OPEN. This switching voltage has a 1V (Typ.) hysteresis and a 4μs (Typ.) mask time to prevent false operation by noise etc. Although this over voltage locked out circuit is built-in, there is a possibility of destruction if the absolute maximum value for power supply voltage is exceeded, therefore the absolute maximum value should not be exceeded. Please be aware that this circuit does not operate during power save mode.

○False operation prevention function in no power supply (Ghost Supply Prevention)

If a logic control signal is input when there is no power supplied to this IC, there is a function which prevents the false operation by voltage supplied via the electrostatic destruction prevention diode from the logic control input terminal to the V_M, to this IC or to another IC's power supply. Therefore, there is no malfunction of the circuit even when voltage is supplied to the logic control input terminal while there is no power supply.

●Power dissipation

○HTSSOP-B24 Package

HTSSOP-B24 has exposed metal on the back, and it is possible to dissipate heat from a through hole in the back. Also, the back of board as well as the surfaces has large areas of copper foil heat dissipation patterns, greatly increasing power dissipation. The back metal is shorted with the back side of the IC chip, being a GND potential, therefore there is a possibility for malfunction if it is shorted with any potential other than GND, which should be avoided. Also, it is recommended that the back metal is soldered onto the GND to short. Please note that it has been assumed that this product will be used in the condition of this back metal performed heat dissipation treatment for increasing heat dissipation efficiency.

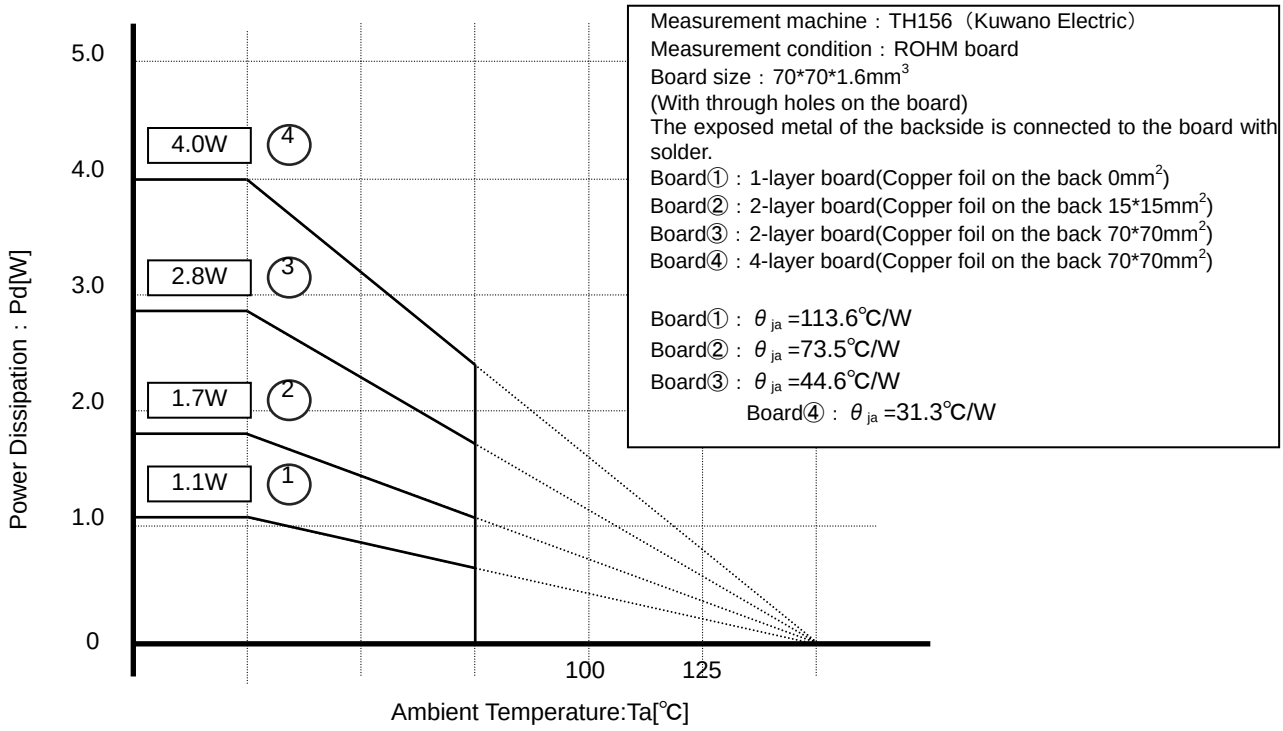


Fig.2 HTSSOP-B24 Derating curve

●Usage Notes

(1) Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

(2) Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

(3) Power supply Lines

Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

(4) GND Potential

The potential of GND pin must be minimum potential in all operating conditions.

(5) Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions. Users should be aware that BD6290EFV has been designed to expose their frames at the back of the package, and should be used with suitable heat dissipation treatment in this area to improve dissipation. As large a dissipation pattern should be taken as possible, not only on the front of the baseboard but also on the back surface.

(6) Inter-pin shorts and mounting errors

When attaching to a printed circuit board, pay close attention to the direction of the IC and displacement. Improper attachment may lead to destruction of the IC. There is also possibility of destruction from short circuits which can be caused by foreign matter entering between outputs or an output and the power supply or GND.

(7) Operation in a strong electric field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

(8) ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

(9) Thermal shutdown circuit

The IC has a built-in thermal shutdown circuit (TSD circuit). If the chip temperature becomes T_{jmax} =150℃, and higher, coil output to the motor will be open. The TSD circuit is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect or indemnify peripheral equipment. Do not use the TSD function to protect peripheral equipment.

TSD on temperature [℃] (Typ.)	Hysteresis Temperature [℃] (Typ.)
175	25

(10) Inspection of the application board

During inspection of the application board, if a capacitor is connected to a pin with low impedance there is a possibility that it could cause stress to the IC, therefore an electrical discharge should be performed after each process. Also, as a measure again electrostatic discharge, it should be earthed during the assembly process and special care should be taken during transport or storage. Furthermore, when connecting to the jig during the inspection process, the power supply should first be turned off and then removed before the inspection.

(11) Input terminal of IC

This IC is a monolithic IC, and between each element there is a P+ isolation for element partition and a P substrate.
This P layer and each element's N layer make up the P-N junction, and various parasitic elements are made up.
For example, when the resistance and transistor are connected to the terminal as shown in figure 3,

○When GND＞(Terminal A) at the resistance and GND＞(Terminal B) at the transistor (NPN),
the P-N junction operates as a parasitic diode.

○Also, when GND＞(Terminal B) at the transistor (NPN)
The parasitic NPN transistor operates with the N layers of other elements close to the aforementioned parasitic diode.

Because of the IC's structure, the creation of parasitic elements is inevitable from the electrical potential relationship. The operation of parasitic elements causes interference in circuit operation, and can lead to malfunction and destruction. Therefore, be careful not to use it in a way which causes the parasitic elements to operate, such as by applying voltage that is lower than the GND (P substrate) to the input terminal.

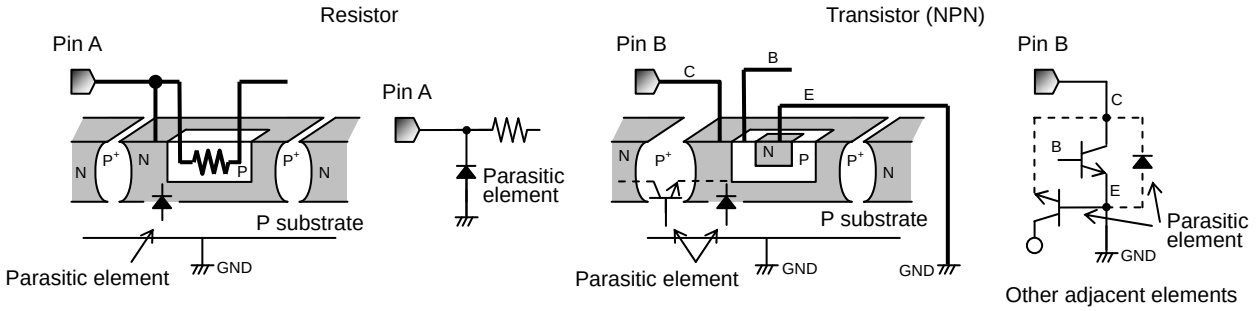


Fig.3 Pattern Diagram of Parasitic Element

(12) Ground Wiring Patterns

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern potential of any external components, either.

(13) TEST Terminal

Be sure to connect TEST pin to GND.

●Ordering part number

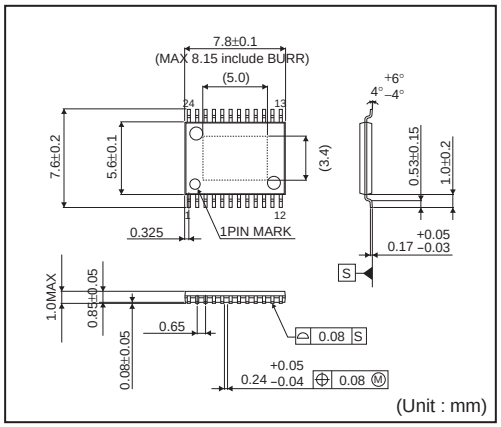
B D 6 2 9 0 E F V	-	E 2

形名

パッケージ
EFV=HTSSOP-B24

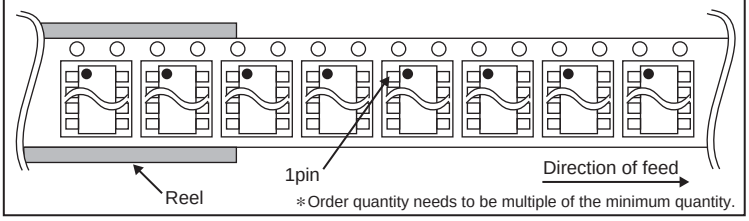
包装、フォーミング仕様
E2: リール状エンボステーピング

HTSSOP-B24



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

No copying or reproduction of this document, in part or in whole, is permitted without the consent of ROHM Co.,Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing ROHM's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from ROHM upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, ROHM shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM and other parties. ROHM shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While ROHM always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/